INVESTIGATIONS ON INVERTED SINE PWM STRATEGIES FOR SYMMETRIC MULTILEVEL INVERTER

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Abstract: *This paper presents about a single phase symmetrical seven level inverter. This topology needs lesser number of switches which reduces the complexity and cost. In this work, the symmetrical reduced switch multilevel inverter is triggered by inverted sine carrier with sinusoidal and trapezoidal reference signals based on the combination of the control freedom degrees. The performance indices like Total Harmonic Distortion, RMS value of output voltage, crest factor and distortion factor were analyzed through the different strategies for various modulation indices. Simulations were performed using MATLAB-SIMULINK.*

Key words: *ISCPDPWM, ISCVFPWM, THD,DF,CF*

1. Introduction

A Multi Level Inverter consists of many steps as a level which dominates the conventional inverter. MLI produces almost sinusoidal voltage with lower harmonics when increasing number of levels. From the basic conventional topologies, cascaded H bridge inverters are most preferred because it needs lesser number of components to achieve the same number of levels. Moreover it requires separate DC sources for each H Bridge, so it is well suited for renewable energy source applications. In multilevel inverter to achieve higher voltages power semiconductor switches and other related devices are should be connected in series manner where switches can be spread out to make the switching losses. It should be noted that multilevel power conversion required more number of switches that increases the cost and complexity in control. The major drawback of multilevel inverters is small voltage steps. They are produced by either individual voltage sources or bank of series capacitors where further voltage balancing is required. To resolve these problems a novel topology with reduced number of switches has been analyzed in this paper.

The performance parameters of multilevel inverter are based on the switching strategy. Lai and Peng [1] suggested high voltage can be achieved by adding multilevel inverter modules. Kazmierkowski and Malesani [2] analyzed the various current control methods for multilevel inverters. Tourkhani et al [3] analyzed the optimal solution for optimal multilevel inverter. Somasekhar et al [4] presented cascaded bridge inverter based an induction motor drive with open end drive system. Bendre et al [5] analyzed the carrier and vector based strategies for inverter. Jeevanandan et al [6] discussed the carrier based PWM methods based on control freedom degree. Gregory and Patangia [7] presented harmonic and switching losses minimized through inverted sine pulse width modulation strategies. Kollensperger et al [8] suggested the controlling strategy of multilevel inverter can be achieved by sinusoidal pulse width modulation (SPWM) or space vector. Franquelo et al [9] described Selective Harmonic Elimination pulse width modulation strategies is best suitable for high-power applications.

Rahim and Selvaraj [10] investigated the grid connected PV system by applying Dual reference modulation strategies in Multilevel Inverter. Zaragoza et al [11] analyzed the hybrid modulation strategies by implementing in neutral point clamped converter. Many researchers [12, 13, 14] have projected pulse width modulation strategies such as sub harmonic PWM, selective harmonic elimination methods are used to obtain best possible least Total Harmonic Distortion. The various research persons show interest in developing a new multilevel inverter with least number of switches. Babaei et al [15] developed new multilevel inverter topologies by incorporating less number of switches when compared to conventional inverters. Ehsan Najafi and Abdul Halim Mohamed Yatim investigated that high frequency switches are used for level generation and low frequency switches for polarity generation in [16].This paper reports a comparative study carried out on inverted sine carrier PWM strategies for new symmetrical MLI by simulation.

2 New Breed Multilevel Inverter

The new single-phase seven-level inverter topology is shown in fig1. The comprehensive structure of the new topology consists of six switches including one H bridge which was used for reversing the voltage

polarity. It has '3' number of isolated identical input voltage. The new multilevel inverter consist three equal sources as input, so the output voltage is:

$$V_o = V_{DC1} + V_{DC2} + V_{DC3} \quad - 1$$

The number output voltage levels in a new inverter are given by,

$$m = 2n + 1 \quad - 2$$

Where n is the number of DC sources

The output voltage levels are generated as follows:

1) $3V_{DC}$: H Bridge switch Q1 and Q2 were turned ON
2) $2V_{DC}$: The switch S2 and H bridge switch Q2 were turned ON.
3) V_{DC} : The switch S1 and H bridge switch Q2 were turned ON.
4) Zero : The H bridge switches Q1 and Q3 are ON, short-circuiting the load.
5) $-V_{DC}$: The H Bridge switch Q3 and switch S2 were turned ON.
6) $-2V_{DC}$: The switch Q3 and switch S1 were turned ON.
7) $-3V_{DC}$: H Bridge switch Q3 and Q4 were turned ON.

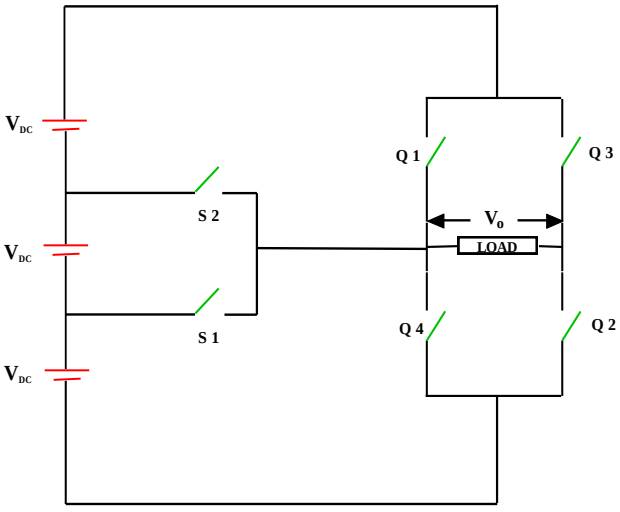

Fig 1 A New Seven Level Inverter Topology

3. Modulation Strategies for Multilevel Inverter

A lot of modulation strategies have been introduced to get optimized output from MLI. Carrier based strategy are most attractive than fundamental switching and space vector modulation strategy because of their controlling ability. To generate m level at the output, bipolar carrier based PWM requires (m-1) carriers. In multicarrier PWM strategy, number of carriers like triangular wave, saw tooth wave and any other design based on CFD where involved with variation in amplitude and frequency. In this work, Inverted Sine Carrier (ISC) PWM was utilized with same and also with variable frequency as a carrier. These ISC were modulated through sine and Trapezoidal reference signals. The Phase Disposition strategy was utilized for same and variable frequency carriers.

The amplitude modulation index is defined as,

$$m_a = 2\,A_m / (m-1)A_c \quad - 3$$

Where

m- no. of levels at the output

A_m - Amplitude of reference wave

A_c - Amplitude of carrier wave

Frequency ratio $m_f = f_c / f_m$ - 4

Where

f_c - frequency of carrier wave

f_m -frequency of reference wave

3.1 Inverted Sine Carrier Phase Disposition (ISCPD) PWM strategy

In phase disposition strategy, all carriers of same frequency f_c and same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous. The reference wave placed at the middle of the carrier set. Fig 2 shows the set of carriers and sinusoidal reference for the ISCPDPWM strategy and Fig 3 shows the set of carriers and trapezoidal reference for the ISCPDPWM strategy

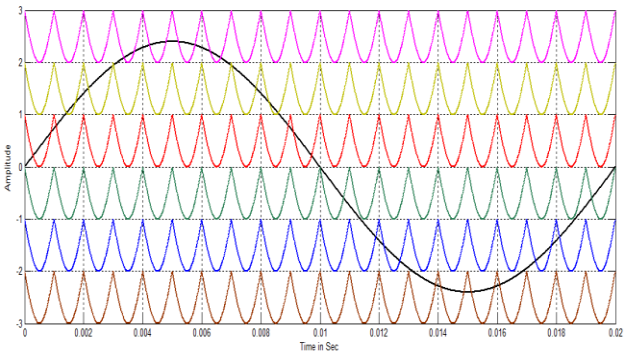

Fig 2 Carrier arrangement for ISCPDPWM Strategy with Sinusoidal Reference (m_a = 0.8)

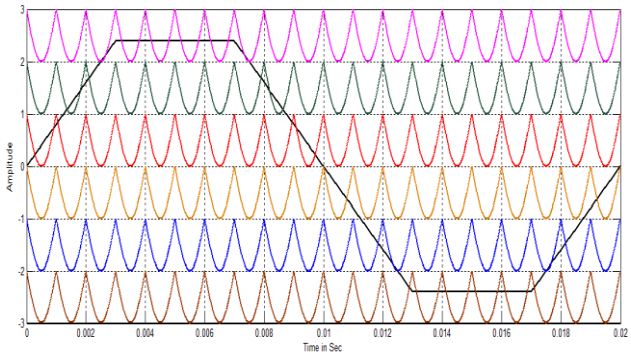

Fig 3 Carrier arrangement for ISCPDPWM Strategy with Trapezoidal Reference (m_a = 0.8)

3.2 Inverted Sine Carrier Variable Frequency Phase Disposition (ISCVFPD) PWM strategy

In variable frequency phase disposition strategy, two different frequencies f_1 and f_2 are used. The alternate carriers (three) are having same frequency and all carriers are having same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous. The reference wave is placed at the middle of the carrier set, where f_1 as 500Hz and f_2 as 1000Hz respectively. Fig 4 shows the set of variable frequency carriers and sinusoidal reference for the ISCVFPDPWM strategy. Fig 5 shows the set of variable frequency carriers with trapezoidal reference for the ISCVFPDPWM strategy

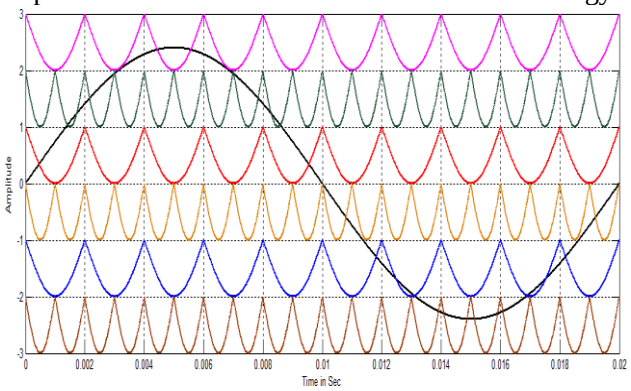

Fig 4 Carrier arrangement for ISCVFPDPWM Strategy with Sinusoidal Reference (m_a = 0.8)

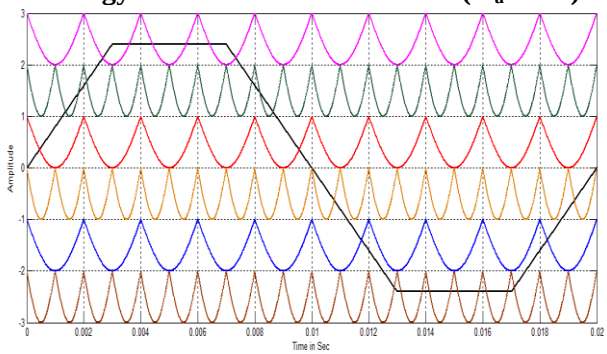

Fig 5 Carrier arrangement for ISCVFPDPWM Strategy with Trapezoidal Reference (m_a = 0.8)

4. Simulation Results

The simulation results have been incurred by employing MATLAB / SIMULINK. Simulations were executed for various values of m_a ranging from 0.7 to 1. The simulated output voltages are shown only one sample value of m_a = 0.8. Figs 6 and 7 display the simulated output voltage of ISCPDPWM with sine and trapezoidal references respectively. Figs 8 and 9 display the simulated output voltage of ISCVFPDPWM with sine and trapezoidal references respectively. Figs 10, 11, 12 and 13 show corresponding FFT plots with above strategies. Fig 14 and Table 1 show the comparison of %THD of output voltage with different PWM strategies for various values of modulation index. The V_{RMS} of fundamental output voltage for different modulation indices are listed in Table 2 and the corresponding graphical representation given in Fig 15. The performance parameters %THD, %DF, CF and V_{RMS} were shown in Table 3 & 4 provides the comparison of %DF and CF of output voltage of above said strategies. From Fig 10 it has been detected that 7^{th}, 8^{th}, 11^{th}, 19^{th} and 20^{th} order harmonics were dominant. It is observed from Figs 11 that, 3^{rd}, 4^{th}, 5^{th} and 20^{th} harmonic energy were dominant. From Fig 12 it has been detected that 3^{rd},5^{th},7^{th}, 8^{th} 10^{th}, 13^{th},14^{th} ,15^{th},18^{th} and 20^{th} harmonic energy were dominant. From Fig 13 it has been detected that 3^{rd},5^{th}, 9^{th},10^{th},11^{th}, 12^{th}, 16^{th},19^{th} and 20^{th} order harmonics were dominant. 20^{th} harmonic energy was dominant in all the strategies. The following parameter values are used for simulation: V_{DC} = 100V, Resistive load = 100ohms.

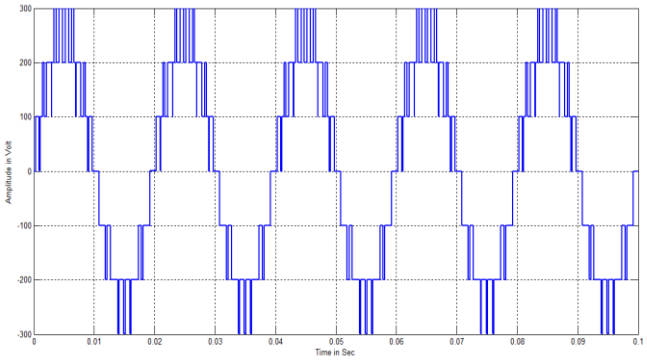

Fig 6 Output voltage generated by ISCPDPWM strategy with Sinusoidal Reference (m_a = 0.8)

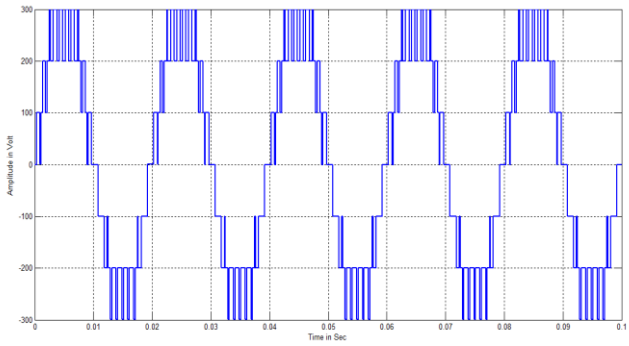

Fig 7 Output voltage generated by ISCPDPWM strategy with Trapezoidal Reference (m_a = 0.8)

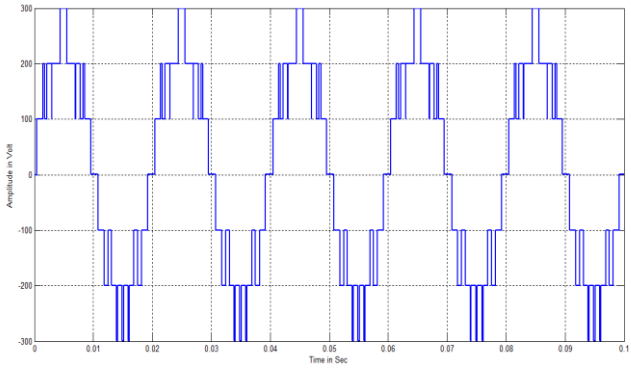

Fig 8 Output voltage generated by ISCVFPWM strategy with Sinusoidal Reference (m_a = 0.8)

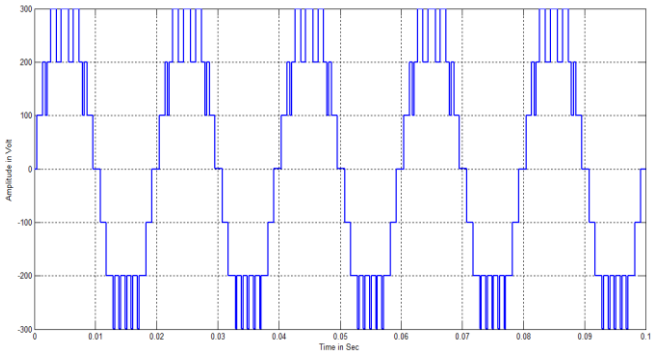

Fig 9 Output voltage generated by ISCVFPWM strategy with Trapezoidal Reference (m_a = 0.8)

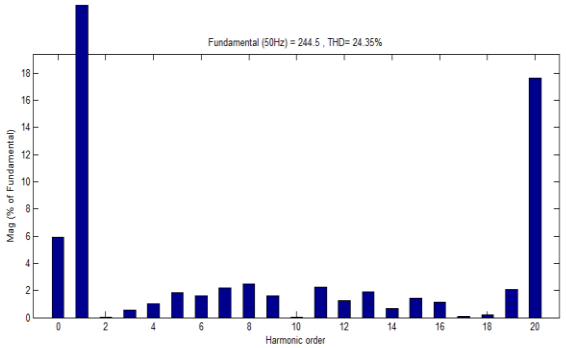

Fig 10 FFT Plot for output voltage of ISCPDPWM Strategy for Sinusoidal Reference (m_a = 0.8)

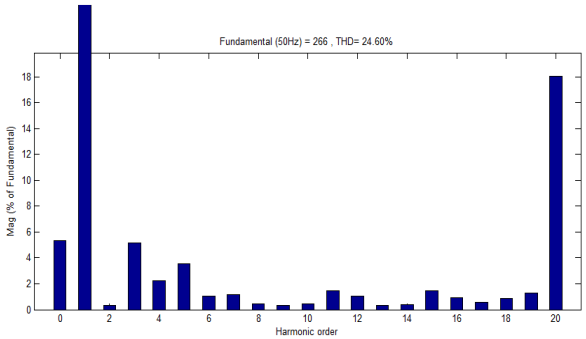

Fig 11 FFT Plot for output voltage of ISCPDPWM Strategy for Trapezoidal Reference (m_a = 0.8)

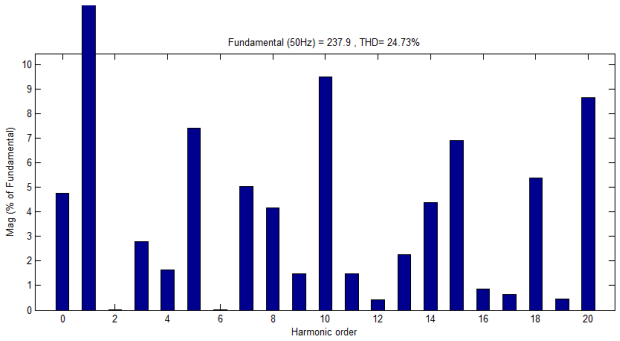

Fig 12 FFT Plot for output voltage of ISCVFPWM Strategy for Sinusoidal Reference (m_a = 0.8)

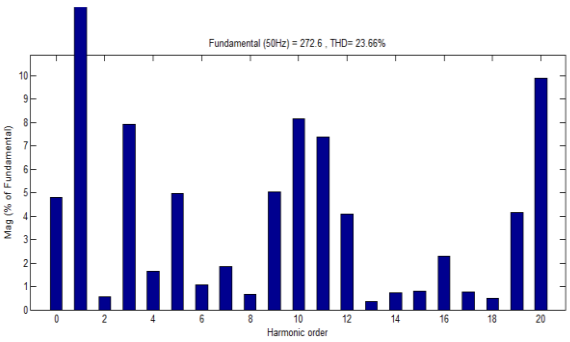

Fig 13 FFT Plot for output voltage of ISCVFPWM Strategy for Trapezoidal Reference (m_a = 0.8)

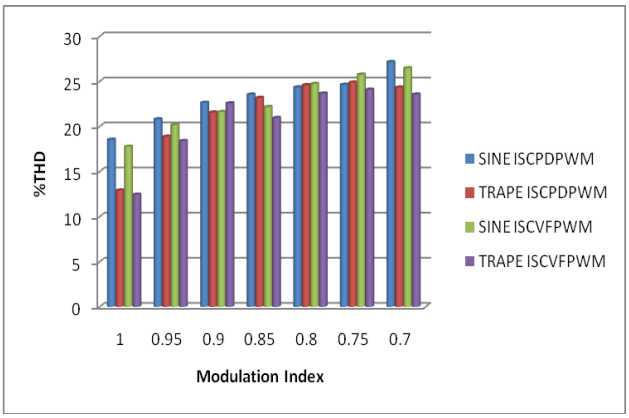

Fig 14 % THD of output voltage v_s m_a

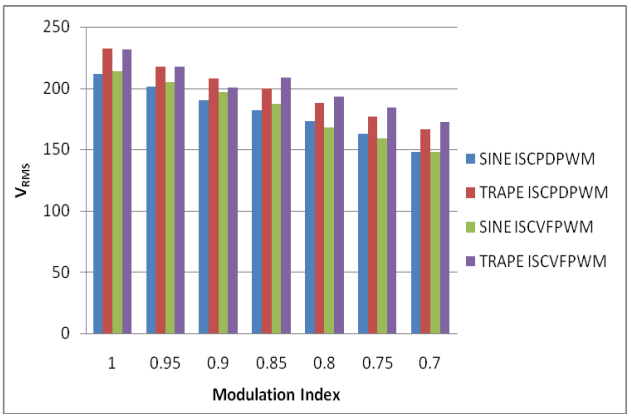

Fig 15 V_{RMS} of output voltage v_s m_a

Table 1: % THD of output voltage for various values of m_a with different ISCPWM strategies.

m_a	ISCPDPWM		ISCVFPWM	
	SINE	TRAPE	SINE	TRAPE
1	18.54	12.91	17.76	12.45
0.95	20.81	18.87	20.17	18.39
0.9	22.63	21.56	21.61	22.58
0.85	23.55	23.19	22.17	20.95
0.8	24.35	24.60	24.73	23.66
0.75	24.63	24.88	25.76	24.09
0.7	27.16	24.33	26.47	23.56

Table 2: V_{RMS} output voltage for various values of m_a with different ISCPWM strategies.

m_a	ISCPDPWM		ISCVFPWM	
	SINE	TRAPE	SINE	TRAPE
1	211.5	232.1	213.9	231.6
0.95	200.9	217.8	204.7	217.7
0.9	189.9	208.1	196.5	200.8
0.85	181.6	199.5	187.4	208.8
0.8	172.9	188.1	168.2	192.8
0.75	162.4	177.0	159.0	184.0
0.7	147.8	166.5	148	172.7

Table 3: % DF of output voltage for various values of m_a with different ISCPWM strategies.

m_a	ISCPDPWM		ISCVFPWM	
	SINE	TRAPE	SINE	TRAPE
1	0.61	1.21	0.45	0.91
0.95	0.38	0.83	0.51	0.73
0.9	0.22	0.78	0.59	0.88
0.85	0.14	0.77	0.63	0.81
0.8	0.14	0.61	0.47	0.92
0.75	0.23	0.45	0.48	0.97
0.7	0.30	0.46	0.35	1.00

Table 4: CF of output voltage for various values of m_a with different ISCPWM strategies.

m_a	ISCPDPWM		ISCVFPWM	
	SINE	TRAPE	SINE	TRAPE
1	1.4141	1.4144	1.4142	1.4140
0.95	1.4141	1.4141	1.4142	1.4143
0.9	1.4144	1.4142	1.4137	1.4138
0.85	1.4140	1.4140	1.4140	1.4137
0.8	1.4141	1.4141	1.4143	1.4139
0.75	1.4144	1.4146	1.4138	1.4141
0.7	1.4147	1.4144	1.4141	1.4145

5 Conclusion

The inverted sine carrier strategies have been studied through new single phase seven level inverter. The performance parameters such as %THD, V_{RMS}, %DF and CF has been measured and tabulated. The inverted sine carrier with same and variable frequency PWM for Sinusoidal and Trapezoidal reference has been analyzed. It has been found that from Table 1 & Table 2, the ISC PWM with trapezoidal reference provides lower harmonics and better DC utilization.

7 References

[1] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[2] M. P. Kazmierkowski and L. Malesani, "Current control strategies for three-phase voltage-source PWM converters: A survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, Oct. 1998.

[3] F. Tourkhani, P. Viarouge, and T. A. Meynard, "A simulation-optimization system for the optical design of a multilevel inverter," *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1037–1045, Nov. 1999.

[4] V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K.Mohapatra, and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 824–836, Jun. 2005.

[5] A.Bendre, G. Venkataramanan, V. Srinivasan, and D. Rosene, "Modeling and design of a neutral point voltage regulator for a three level diode clamped inverter using multiple carrier modulation," *IEEE Trans. Ind. Electron.*, vol. 53, no. 3, pp. 718–726, Jun. 2006.

[6]Jeevananthan, S.; Madhavan, R.; Suresh Padmanabhan, T.; and Dananjayan, P. (2006). State-of-the-art of multi-carrier modulation strategies for seven level inverter: A critical evaluation and Novel submissions based on control degree of freedom. *IEEE International Conference on Industrial Technology, Conf. Rec.:* 1-4244-0726-5/06, 1269-1274

[7] Gregory, D. Patangia, H. "A Novel Multilevel Strategy in SPWM Design" Industrial Electronics. IEEE International Symposium, . ISIE 2007, pp.515-520.

[8] P. Kollensperger, R. U. Lenke, S. Schroder, and R. W. De Doncker, "Design of a flexible control platform for soft-switching multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1778–1785, Sep. 2007

[9] L. G. Franquelo, J. Napoles, R. C. Portillo Guisado, J. I. Leon, and M. A. Aguirre, "A flexible selective harmonic mitigation strategy to meet grid codes in three-level PWM converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6 , pp. 3022–3029, Dec. 2007

[10] Rahim N. A. and Selvaraj J., ".Multilevel Inverter with Dual Reference Modulation Strategy for Grid-Connected PV System" IEEE Power and Energy Society General Meeting, pp. 1-8,2009.

[11] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation strategy for the neutral point clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 294–304, Feb. 2009.

[12] A. Kaviani, S. H. Fathi, N. Farokhnia, and A. Ardakani, "PSO, an effective tool for harmonics elimination and optimization in multilevel inverters," in *Proc. 4th IEEE Conf. Ind. Electron. Appl.*,May 25–27, 2009, pp. 2902– 2907.

[13] W.Fei, X.Ruan, and B. Wu, "A generalized formulation of quarter-wave symmetry SHE-PWM problems for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1758–1766, Jul. 2009.

[14] M. T. Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009.

[15] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Convers. Manage.*, vol. 50, no. 11, pp. 2761–2767, Nov. 2009.

[16]Ehsan Najafi, Abdul Halim Mohamed Yatim, " Design and Implementation of a New Multilevel Inverter Topology"*IEEE Trans. Ind. Electron.*, vol. 59, no. 11 pp. 4148–4154, Nov. 2012.