IMPROVED PERFORMANCE OF LINEAR QUADRATIC REGULATOR plus FUZZY LOGIC CONTROLLER FOR POSITIVE OUTPUT SUPER-LIFT LUO-CONVERTER

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Abstract: *This paper study on the analysis, design and implementation of linear quadratic regulator (LQR) plus fuzzy logic controller (FLC) for super lift Luo-Converter (SLLC)) for purposes needing the constant power source in battery operated portable devices, floppy disk drives, hard disk drives, LED TV, physiotherapy medical instrument, lap-top computers, mobile phones and communication interface in robot system applications etc.,. In this case, the positive output elementary SLLC (POESLLC) is considered for study. The POESLLC is variable structure system (VSS) and its dynamic performance become non-linear in nature. The conventional controllers are not able to get better the dynamic performance in line as well as load disturbances. In an effort to enhance the dynamic performance, output voltage and inductor current regulations in large input supply voltage and load resistance variations, a LQR plus FLC is developed. The LQR is designed for the naturally VSS of the POESSLLC using the state-space average based model. The controller formation of this converter consists of two loops namely, inner current loop and output voltage loop. Here, LQR is act as inner current loop for regulating the inductor current of this converter, whereas the FLC is adopted as an outer loop for controlling the output voltage of same converter. The FLC is designed based on the converter activities and qualitative linguistic control rules. The performance of this converter using LQR plus FLC is verified at various operating regions viz. transient region, line and load variations, and steady state region for building both MATLAB/Simulink and prototype field gate programmable array (FGPA) models in comparisons with LQR plus linear controller. The results and time domain specifications analyze are presented to prove the adept of developed controller in different regions.*

Keyword: *DC-DC power conversion, super lift Luo-converter, linear quadratic regulator, fuzzy Logic controller and state-space average model.*

I. INTRODUCTION

The exponential development in usage of the portable electronic devices and other battery operated appliances has added enormous research scope to DC-DC converter domain. A several number of DC-DC converter structures have been developed and researched [1-6]. The converter structures which are different concept, performance and application suitability and assembled into six generations [7]. The fundamental based voltage stepping-up converters namely, boost and buck-boost converters, which generate the pulsating output current, the low voltage transfer gain, the produce moderate efficiency and the generate the more output voltage/inductor current ripples. To rectify these problems, the Luo-Converters (LC) has been developed [6-7]. Mainly LC is classified into three techniques namely, voltage lift (VL), super-lift (SL), and ultra-lift (UL). In VL, the output voltage transfer gain improves in arithmetic progression, whereas the output voltage transfer gain increases in geometric progression for SL. The UL has combined characteristics of both the VL and the SL. The feed-back controller design for LC is challenge role for design engineers because of its no-linearity structure. In this paper, one of the techniques of LC is considered for controller design study namely, positive output elementary super lift Luo-Converter (POESSLC). The most two important classical modeling approaches for DC-DC converters namely, switching signal flow graph (SSFG) and state space averaging method (SSAM) [8-9]. Still, among these methods SSAM has applied for many of power converter. The validation of classical linear controllers for conventional DC-DC converters has been addressed [10-11]. Still, these control methods are very insightful to circuit components modifications, changing from ON/OFF states, large line and load variations etc.

The sliding mode controller (SMC) for the positive output elementary LC has been discussed [12]. However, the results of the converter has produced large peak overshoots and long settling time using controller at different operating conditions. The SMC with maximum power point tracing for DC-DC converters has been reported [13]. But, the results of the LCs have produced excellent performance except the small chattering. The SMC plus fuzzy logic controller (FLC) for positive output elementary split inductor-type boost converter was presented [14]. Still, in this article studied only software simulation study under various operating stages. Experimental verification of DC-DC boost converter using PI compensator has been well executed [15]. From this article, the output voltage of the converter has generated more

overshoots and long settling time during line and load variations. The SMC with fractional order differentiation for unstable time delay systems has been well organized [16]. However, the results are produced huge overshoots during step-change variations. The fixed switching frequency based SMC for various LCs has been discussed [17]. Still, the results of these converters using SMC have produced poor time domain specifications (TDS) during large line and load variations. The hysteresis band based SMC for boost converter has been presented [18]. However, the results of this converter has produced chattering and produced poor TDS using this control method.

Linear quadratic regulator (LQR) is one of the methods of optimization cost function/performance index. For that reason, the designer can weigh, which states are more imperative in feed-back control action to look for appropriate performance. This kind of quality of LQR is initiated by many researchers and it is more adopted for many of the power electronics converters. The pole placement approach is used for selection of performance index has been well presented [19]. But, this approach depends on the exact placement of the feed-back poles. The cost function is evaluated from a basic controller with help of frequency domain approach has been reported [20]. However, the problem of this method is taking long time for calculations. The optimal possible controller recommends a systematic way of designing a LQR and issues of where to place the closed loop poles does not occur and is robust to converter circuit parameter, input supply voltage and load modifications.

The fuzzy logic controller (FLC) is a form of heuristic-reasoning based expert-knowledge customary control method. The FLC could not need an exact model of the systems or complex calculations. It is easy because FLC relies on the designer's accepting of the systems behaviors and is based on the qualitative linguistic control rules. The inductor current and load voltage regulation of the various groups of DC-DC converters has been clearly addressed [21]. From these surveys, it is obviously demonstrated that the first-rate output voltage regulation for assorted DC-DC converters with help of FLC in enormous input voltage and load variations. These above addressed issues are rectifying by using the LQR plus FLC.

Therefore, in this article, it is developed to a design of a LQR plus FLC for POESLLC worked in continuous conduction mode (CCM). The state space dynamic equations of this converter are derived at beginning and then the LQR controller parameters are designed to control the inductor of the converter. Here, the FLC is utilized to control the load voltage of the converter and its rules are designed based on the same converter characteristics. The performance of the POESLLC using this controller is validating at various working conditions viz. appropriate selection of the controller gains and fuzzy rules. The major impacts of LQR are realization with variable frequency (within the boundary limit) and produced fastest dynamic performances.

The organization of this paper is as follows. Section 2 presents the circuit operation and state-space average modeling of the POESLLC. The complete systematic step by step design procedure of LQR plus FLC for the POESLLC is presented in sections 3. The results of the POESLLC using ROLQR plus FLC at the various operating regions are discussed in sections 4,5. The conclusions are listed in sections 6.

II. Design of POESLLC

A. Operation and state space averaging of POESLLC

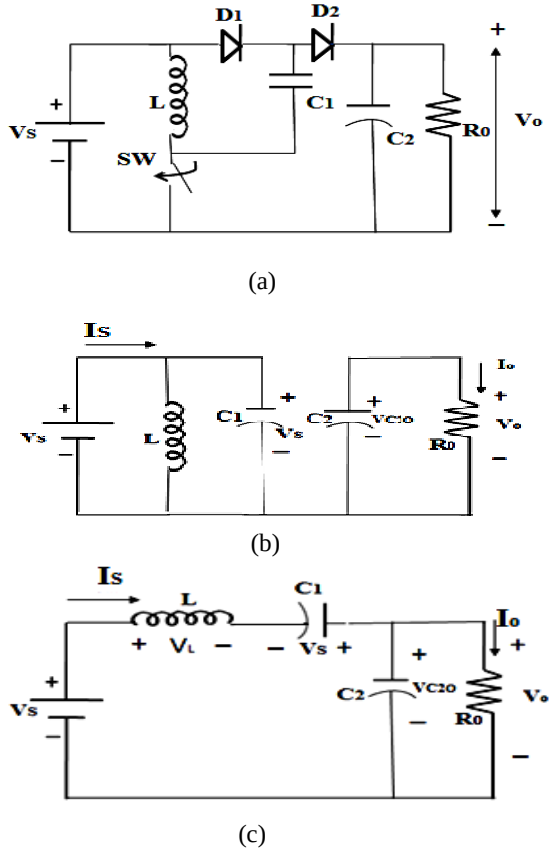


Fig.1 Power circuit of POESLLC, (a) Topology, (b) Equivalent circuit during state 1 operation, (c) Equivalent circuit during state 2 operation.

The topology of the POESLLC is exposed in Fig.1 (a). From this topology, V_s is a source voltage, SW is the n-channel power MOSFET switch, D_1 and D_2 are the freewheeling diodes, C_1 and C_2 are the energy storage capacitors, L is storage inductor, V_o is the output voltage and R_o is the load resistance. Assume that the components are ideal and also the POESLLC is operating in CCM. To analyze the working of the POESLLC, the circuit can be divided into two states, viz. the switch-ON and the

switch-OFF. Fig.1 (b) and Fig.1(c) show the two operating interval of the POESLLC [3].

In state 1 operation, the switch SW is in closed state, the diode D_1conducts. The capacitor C_1 is charged by level of V_S in short span and this capacitor voltage is assumed a constant value. The current through the inductor i_L dependent with V_S. The output capacitor, C_2 offers the energy to the load. The equivalent circuit of POESLLC in stage 1 operation is shown in Fig. 1(b). The state space equation can be expressed as (1)

$$\begin{cases} L\dfrac{di_L}{dt} = V_S \\ C_2\dfrac{dV_O}{dt} = -\dfrac{V_O}{R} \end{cases} \quad \text{Switch ON} \qquad (1)$$

During the state 2 operation, the switch SW is in open state, diode D_2 conduct and the inductor current decreases with voltage (V_o - $2V_{in}$) to provide energy to C_2 and load branch. The equivalent circuit of POESLLC in state 2 is shown in Fig.1(c). The state space equation can be emblazoned as (2)

$$\begin{cases} L\dfrac{di_L}{dt} = 2V_S - V_O \\ C_2\dfrac{dV_O}{dt} = i_L - \dfrac{V_O}{R} \end{cases} \quad \text{Switch OFF} \qquad (2)$$

Using the capacitor charge balance rule on C_1, the equation (3) for entire switching time period can be written. Where u is the status of the switch (d=1 when the switch is ON, and d=0 when the switch is OFF).

$$dC_1\frac{dV_{C1}}{dt} + (1-d)i_L = 0 \qquad (3)$$

As there are two capacitors in the POESLLC, which are V_{C1} = V_{in}, V_o, it is only require to select as a state space variable except V_{in}. Jointly with inductor current $i_{L1,}$ all state space variables of the converter are selected for the inductor current i_{L1}, and voltage V_o respectively x_1, and x_2. Utilizing (1), (2), and (3), the reduced-order state-space average modeling of the POESLLC can be reached as expressed by (4).

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\ \dfrac{1-d}{C_2} & -\dfrac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \dfrac{2-d}{L_1} \\ 0 \end{bmatrix} V_{in}$$
$$Y = [0 \quad 1] \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} \qquad (4)$$

Where, *A, B, C* and *D* are averaged reduced order system state space matrices.

$$A = \begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\ \dfrac{1-d}{C_2} & -\dfrac{1}{RC_2} \end{bmatrix},\ B = \begin{bmatrix} \dfrac{2-d}{L_1} \\ 0 \end{bmatrix},\ C = [0\ 1],\ D = [0\ 0] \qquad (5)$$

B. Design calculation of values of POESLLC

The design starts with mathematical computations that should be explicated in detail from the POESLLC specifications listed in Table 1.

The design process consists of six stages that should be repeated easily to this converter as follows.

Stage 1: Select the duty cycle d for POESLLC, which is calculated by using the expression

$$\frac{V_o}{V_{in}} = \frac{2\text{-}d}{1\text{-}d},\ d = \frac{2V_{in} - V_o}{V_o - V_{in}},\quad d = \frac{2*12-36}{36-12} = 0.5 \qquad (6)$$

Stage 2: Calculate the average output current by using the equation (7)

$$I_o = \frac{V_O}{R_O} = \frac{36}{50} = 0.72\text{A} \qquad (7)$$

Stage 3: Obtain the output power with help of the equation

$$\begin{aligned} P_o &= V_O I_O \\ P_o &= 36*0.72 \\ P_o &= 25.92\ \text{W} \end{aligned} \qquad (8)$$

Stage 4: Select the efficiency of the circuit and let it be 91.79 % in this case. Using the efficiency value, the value of the input power can be calculated by using the equation (9).

$$\eta = 91.79\%,\quad P_{in} = P_o/\eta,\ P_{in} = 25.92/0.9179$$
$$P_{in} = 28.238\ \text{W} \qquad (9)$$

Stage 5: Evaluate the average input current using the equation (10)

$$I_{in} = \frac{P_{in}}{V_{in}} = \frac{28.238}{12},\ I_{in} = 2.353\text{A} \qquad (10)$$

Stage 6: Select the inductor current ripple $\Delta i_L = 0.6\text{A}$ by using the nominal switching frequency mentioned in the Table. 1, and calculate the necessary value of the inductor using the equation (11).

$$L=\frac{V_{in}}{f_s \Delta i_L} d,\ L=\frac{12}{100e^3*0.6}*0.5,\ L=100\mu H \quad (11)$$

Stage 6: Choose the capacitor voltage ripple $\Delta V_o = 0.12\,V$ by using the nominal switching frequency specified in the Table. 1 and calculate the essential value of the capacitor using the equation (12).

$$C_2=\frac{(1-d)V_o}{f_s \Delta V_o R},\ C_2=\frac{(1-0.5)*36}{100e^3*0.12*50},\ C_2 = C_1 = 30\mu F \quad (12)$$

The design specifications are substituted in (5) and after using the phase-variable transformation, *A*, *B*, *C*, and *D* matrices becomes

$$A=\begin{bmatrix} 0 & -5000 \\ 11000 & -16666.67 \end{bmatrix},\quad B=\begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad (13)$$

$$C=[165000000 \quad 0],\ D=[0 \quad 0]$$

Table 1. The designed specification of the POESLLC (Power Supply for LED TV)

Parameters name	Symbol	Value
Input Voltage	V_S	12V
Output Voltage	V_o	36V
Inductor	L	100µH
Capacitors	C_1, C_2	30 µF
Nominal switching frequency	f_s	100kHz
Load resistance	R_o	40Ω -70Ω
Output power	P_o	25.92 W
Input power	P_{in}	28.238 W
Average input current	I_S	2.353A
Efficiency	η	91.8%
Average output current	I_o	0.72A
Peak to Peak Inductor Current Ripple	Δi_L	0.6 A
Peak to Peak Capacitor Ripple	ΔV_o	0.12 V

III. DEVELOPMENT OF FEED-BACK CONTROLLERS FOR THE POESLLC

The function of this section is to deal about the feed-back controller for the POESLLC. The LQR plus FLC arrangement for the POESLLC converter is revealed in Fig. 2. It consists of two control loops such as an inner current loop that acts as LQR for regulate the inductor current i_L, and the outer voltage loop of FLC acts as to regulate the output voltage of the POESLLC and, also to minimizes steady state error. The error e_1 is measured from the output voltage that measured error signal is given as input to the FLC and the output fix the average power loss. The input for the LQR is current error e_2. The signal *u* indicate the control signal that is given to output of LQR , which in turn sets the newfangled duty ratio of the switching pulse for driving the power MOSFET switch of the POESLLC.

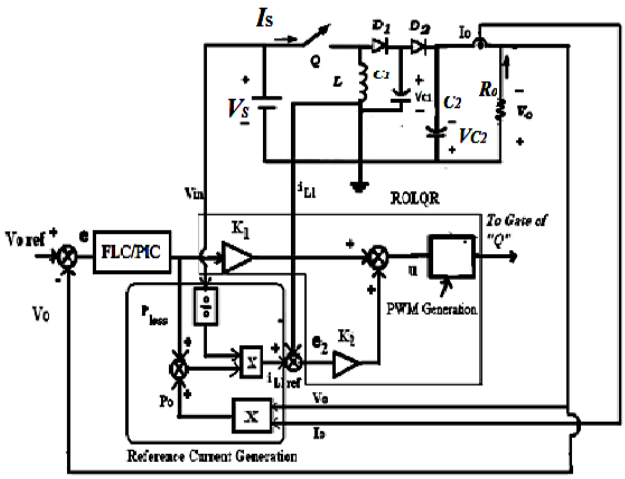


Fig 2. Control structure of the POESLLC.

A. Generation of reference current

The reference inductor current of POESLLC is derived by with help of the equations (14) is

$$i_{Lref}=\frac{P_{loss}+P_o}{V_S} \quad (14)$$

Where,

$$P_o = V_o I_o$$

V_O = output power in W

I_o = output current in A

$$P_{loss}=K_p e_1 + K_i \iint e_1 dt$$

$$e_1 = V_o - V_{oref}$$

In (14) equation, it clearly found that the term P_{loss} mentions the converter ON/OFF and ohmic losses. In consequence of losses in given model, the fall of capacitor output voltage, while the capacitor output voltage falls down upto the reference output voltage, the converter cannot be able to follow the reference inductor current narrowly. Hence, suitable FLC is applied that control the capacitor output voltage to the reference output voltage level, which is said as equation (14). The term P_o signifies the load power, which is the product of the load voltage and the load current of the

given system.

B. Design of LQR

The theory of optimize the control is complexity with operating a dynamic system at smallest amount of cost. The time- invarying LQR is applied as tracking current regulator. In this case, LQR controller gain matrix for the POESLLC is evaluated by suitable selection values of R and Q (weight matrix). The values for Q and R matrices are

$$Q=\begin{bmatrix}2.16 & 1.1\\ 1.1 & 1000\end{bmatrix},\quad R=[1] \tag{15}$$

The Q matrix is preferred in such a way that highest weightage is given to inductor current, successively that inductor current of the POESLLC is controlled very efficiently using LQR controller. The Q and R matrixes would be positive semi-definite and positive definite, correspondingly, which are selected such that the scalar quantity x^TQx is all the time positive or zero at every time t for the all functions x(t), and the scalar quantity u^TRu is always positive at each time t for all values of u(t). In terms of eigen values, the eigen values of Q would be positive, whereas those of R could be positive. For a continuous time model the state-feedback control law $u = -K_F x$ minimizes the quadratic cost function;

$$J\left(x(.),u(.)\right)=\frac{1}{2}\int_{t_o}^{t_f}(x^TQx+u^TRu)\,dt \tag{16}$$

Subject to the system dynamics

$$\dot{X}=AX+BU \tag{17}$$

For the developed converter, the quadratic cost function is found after substituting the values of X, Q, R in equation (16)

$$\int_{t_o}^{t_f}[(2.16x_1^2+2x_1x_2+1000x_2^2)+u^2]dt \tag{18}$$

The control law is found to be

$$u=-R^{-1}B^TKx=u=-K_Fx \tag{19}$$

Where, K_F is the feed-back controller gain matrix and K is the return function matrix. The unknown coefficients of the return function matrix are found by solving the Ricatti equation.

$$K=Q+A^*PA-A^*PB(R+B^*PB)^{-1}B*PA \tag{20}$$

On solving equation (20), the return function matrix K is found to be

$$K=\begin{bmatrix}K_{11} & K_{12}\\ K_{21} & K_{22}\end{bmatrix}=\begin{bmatrix}2.2 & 1.1\\ 1.1 & 1000\end{bmatrix} \tag{21}$$

On substituting the value of K matrix in the equation, $K_F = -R^{-1}B^TK$ the feedback gain matrix K_F is obtained. It is found to be [1.1 1000]

Therefore, the control law becomes

$$u=-1(x_{1ref}-x_1)-1000(x_{2ref}-x_{ref}) \tag{22}$$

Once again the equation (22) becomes expressed as (23)

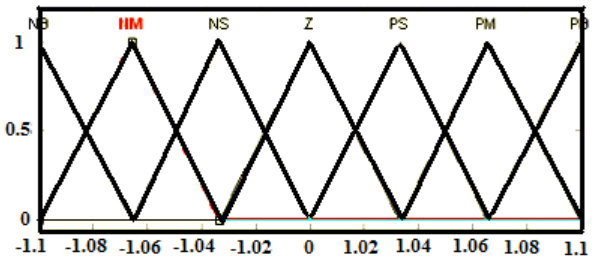
$$u=-(K_1e_1+K_2e_2) \tag{23}$$

Where, K_1= 1.1 and K_2= 1000

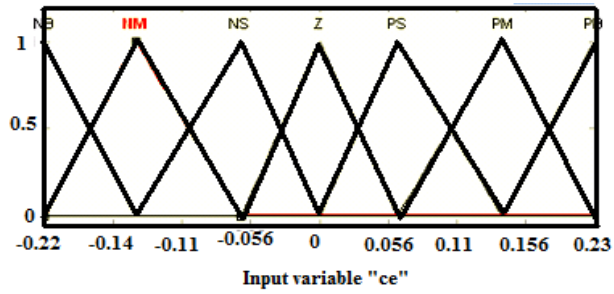
C. Design of FLC

This section discusses about the FLC design of the POESLLC. Here, the FLC is included as an outer loop, which is applied to control the power switches of the POESLLC. The inputs and output of the FLC is exposed in Fig. 3 (a) to (c). The voltage error (e) and its change in error (ce) of POESLLC is applied as input of FLC and the output is o (mark the reference current for the inductor). For suitability, the numerical ranges of the inputs and output of the FLC will be uniform and engraved as follows: e = [-1.1 -1.08 -1.06 -1.04 -1.02 0 1.02 1.04 1.06 1.08 1.1], ce = [-0.22 -0.14 -0.11 -0.056 0 0.056 0.11 0.156 0.23] and o = [-1 -0.067 -0.0433 0 0.0433 0.0767 1] and its corresponding fuzzy sets are [NB, NM, NS, Z, PS, PM, PB] where, NB (negative big), NS (negative small), Z (zero), PS (positive small), PM (positive medium), PB (positive big), respectively. The membership functions of the e, ce, and o are shown in Fig. 3.

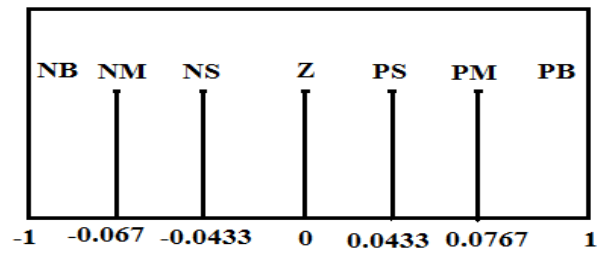
The selection of the FLC rules is entirely based on the performance activities of the POESLLC. In this article, 49 rules are framed (refer the Table 2). Then, the weighted average method method is used as defuzzification process to complete the fuzzy work design.



(a)



(b)



(c)

Fig. 3 Membership's functions of FLC, (a) error (e), (b) change in error (ce), and (c) output (o).

Table 2. Fuzzy rules of POESLLC

E / CE	NB	NM	NS	Z	PS	PM	PB
NB	NB	NM	NB	NB	NM	NS	Z
NM	NM	NM	NB	NM	NS	NM	PS
NS	NB	NB	NS	NS	Z	PS	PM
Z	NB	NM	NS	Z	PS	PM	PB
PS	NM	NS	Z	PS	PS	PM	PB
PM	NS	Z	PS	PB	PM	PM	PB
PB	Z	PS	PS	PS	PB	PB	PM

Output (o): NB=-1; NM= -0.067; NS= -0.0433; Z=0; PB=1; PM= 0.0767; PS=0.0433

4. SIMULATIONS RESULTS

The main function of this section is to deals about the simulation results of the POESLLC with LQR plus FLC in comparison with LQR plus PDIC at different operating condition with specifications are listed in Table 1.

A. Start-up transient

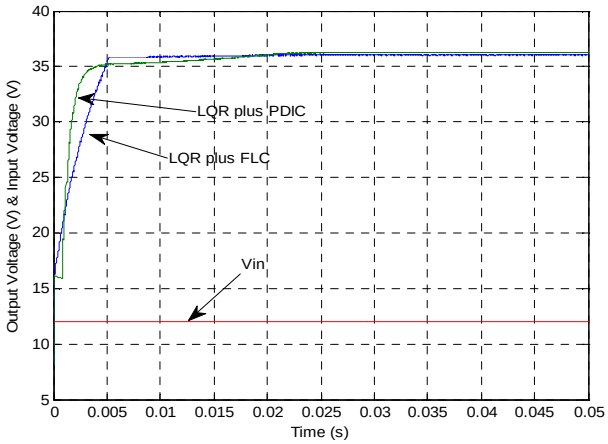


Fig. 4 Simulated output voltage responses of POESLLC using controllers in nominal input voltage and load resistance.

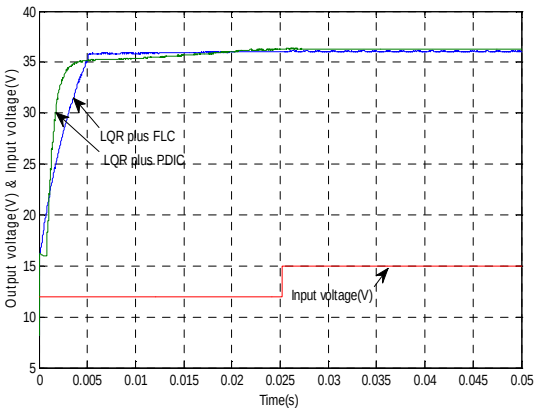
Fig. 4 show the simulated output voltage responses of the POESLLC for the nominal input voltage and load resistance using LQR plus FLC and LQR plus PDIC in start-up transient. It can be seen that the output voltage of the POESLLC using LQR plus FLC has a negligible start-up overshoot and fast settling time, whereas the same model using LQR plus PDIC has null overshoots and quick settling time during transient regions.

B. Line Variation

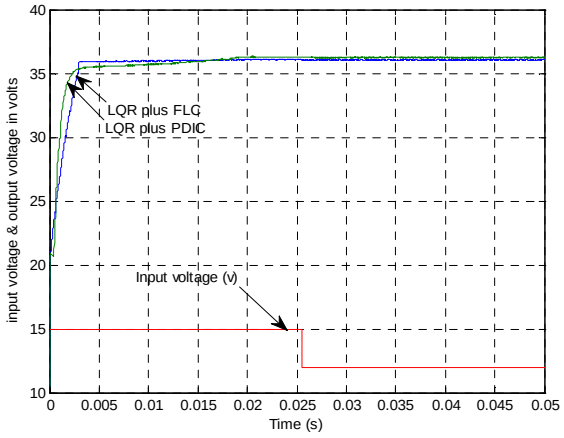
Fig. 5 (a) indicates the simulation responses of the output voltage and input voltage of the POESLLC using the LQR plus FLC for input voltage step change from 12V to 15V at time = 0.026s. From this figure, it is clearly initiate that both the simulation responses of output voltage of the POESLLC with the designed LQR plus FLC has little overshoot and small settling time, but the same system using LQR plus PDIC has produced overshoots and long settling time.

Fig.5 (b) show the simulation responses of the output voltage and input voltage of the POESLLC using the LQR plus FLC for input voltage step change from 15V to 12V at time = 0.026s. It can be observed that the simulation responses of output voltage of the POESLLC using LQR plus FLC have small overshoot and settling time, while the same system using LQR plus PDIC has produced overshoots and long settling time. From the

Fig.5, it is clearly showed that the simulated results of a designed controller are presented enriched performance during the line variation.



(a)

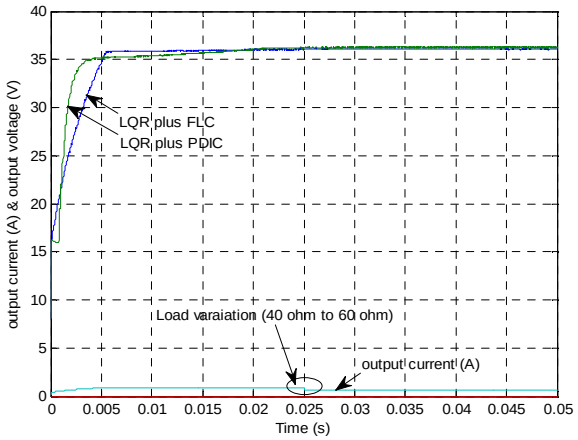


(b)

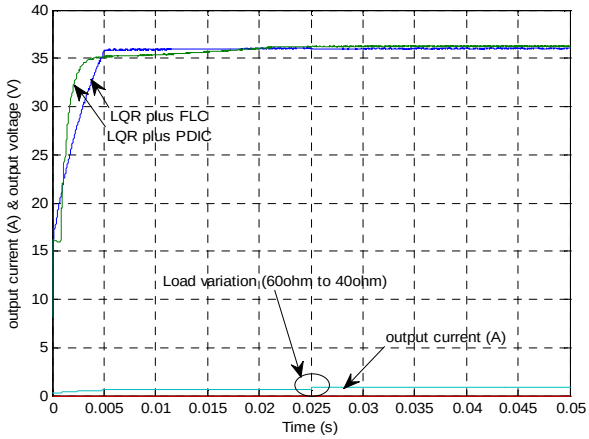
Fig. 5 Simulated output voltage responses of the POESLLC using controllers, (a) for input voltage variation from 12V to 15V, (b) for input voltage variation from 15V to 12V.

C. Load Variation

Fig. 6. (a) and Fig. 6. (b) show the simulation responses of output voltage and load current of the POESLLC using controllers for load change from 40Ω to 60 Ω and 60Ω to 40Ω at time = 0.025s. It can be understood that the simulation results of the output voltage of the POESLLC using LQR plus FLC has a little overshoot as well as fast settling time, whereas the LQR plus PDIC for same model has produced overshoots and long settling time. From the Fig.6, it is clearly implicit that the simulation results relate the close agreement with load variation using the designed controllers.



(a)



(b)

Fig.6 Simulated output voltage responses of the POESLLC using controllers, (a) for load resistance variation from 40Ω to 60Ω , (b) for input voltage variation from 60Ω to 40Ω.

D. Steady state region

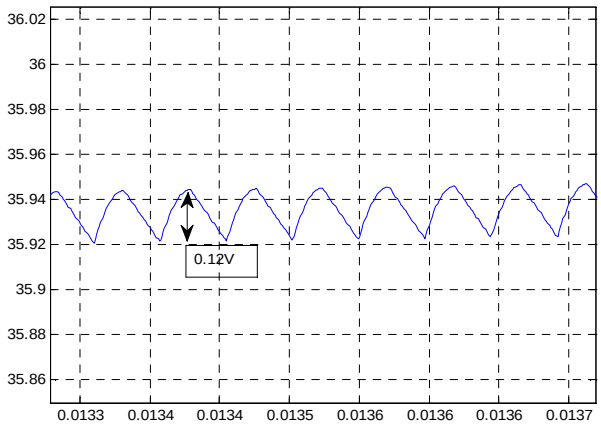
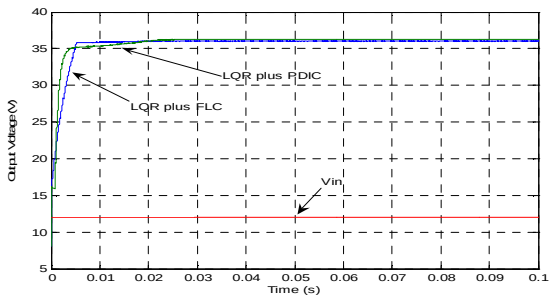


Fig.7 Simulated output voltage responses of the POESLLC using controllers in steady state region.

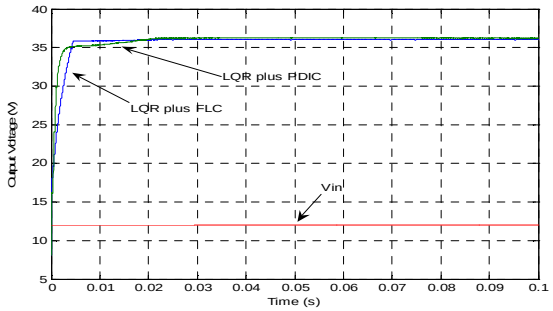
Fig.7 shows the simulated instantaneous output ripple voltage of the POESLLC in the steady state region using a LQR plus FLC. It is evident from the figure that the output voltage ripple is very small about 0.015V for the average switching frequency of 100 kHz.

E. Circuit components variations

Fig. 8(a) represents the simulation response of output voltage and output current of the POESLLC using a LQR plus FLC and LQR plus PDIC for inductor L_1 variation from 100µH to 600µH. It could be found that the change does not impact the POESLLC performances due to a skilled designed controller. A fascinating result is shown in Fig. 8(b). It indicates the simulation response of output voltage and output current of the POESLLC with designed controllers for the change in capacitors ranges from 30µF to 100µF. It can be seen that the designed LQR plus FLC and LQR plus PDIC are very effective in suppressing the effect of capacitance variation except that a small overshoot and fast settling time.



(a)



(b)

Fig.8 Simulated output voltage responses of POESLLC using controllers in circuit components variations, (a) for inductor L_1 variation from 100µH to 600µH, (b) for the change in capacitors ranges from 30µF to 100µF.

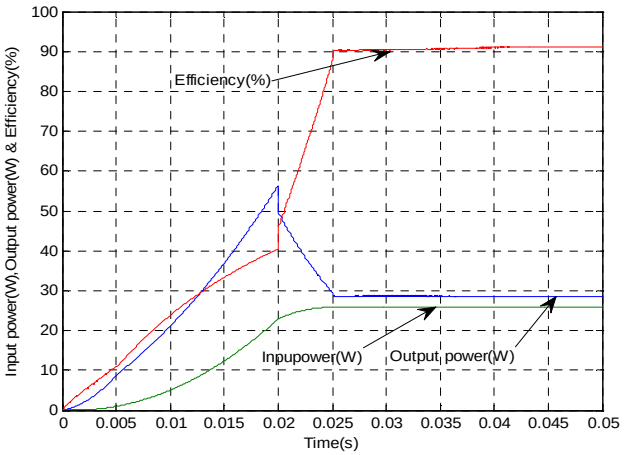


Fig.9 Simulated performance responses of POESLLC using LQR plus FLC.

Fig. 9 shows the simulated efficiency, input and output powers of POESLLC using LQR plus FLC. It is evidently showed that the %efficiency of the converter various from 82 to 92 %. In addition, the same model can be work in large input and output power rating with require of high level design.

5. EXPERIMENTAL RESULTS

The aim of this section is to discuss about the experimental results of the POESLLC with LQR plus FLC. The validation of the system performance is done for five different conditions through start-up transient, line variation, load variation, steady state region and also circuit components variations. The laboratory prototype is performed on the POESLLC circuits with specifications listed in Table 1. The experimental block diagram model of the POESLLC with the implemented ROLQR plus FLC is shown in Fig. 10.

The details of the power circuits are as follows:

Q	IRFP 260 (MOSFET);
D_1 - D_2	FR306 (Diodes);
$C_1 – C_2$	30 µF/200V (Electrolytic and plain polyester type)
L_1	100µH/5A (Ferrite Core)

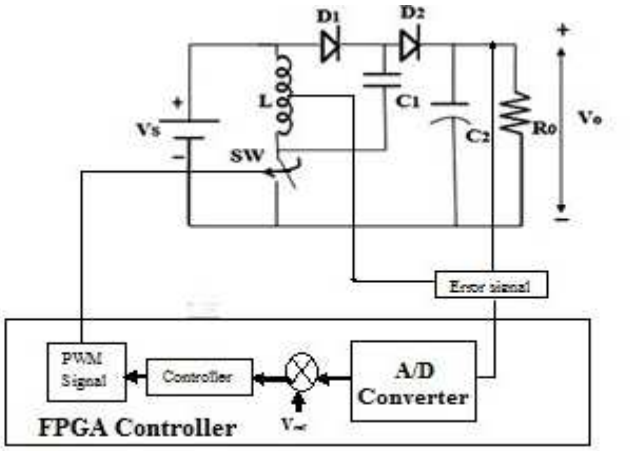
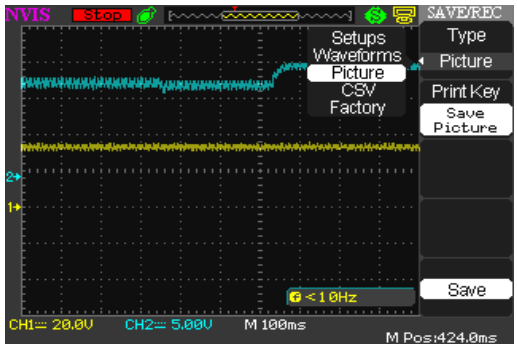


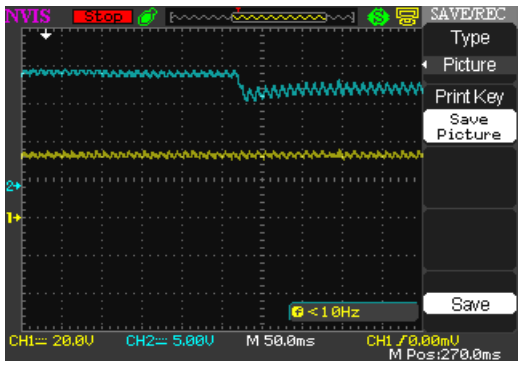
Fig.10 Experimental block diagram of POESLLC with controller.

The parameters of the FLC controller are given as NB=-1; NM= -0.067; NS= -0.0433; Z=0; PB=1; PM= 0.0767; PS=0.0433 calculated in the previous section. The controller parameter of LQR plus FLC is executed in FPGA controller platform (refer the Fig. 10). In closed loop operation, measured values of the input voltage, the inductor current and output voltage are scale down to slighter than ± 10V with help of signal conditioning circuit and isolation circuit. The ADC signals are processed by designed controller algorithm to compute the new duty cycle of power switch SW. The PWM pulse is derived from FPGA controller and it is applied to trigger MOSFET of the POESLLC using opto-coupler and driver IR2110. The main aim of the opto-coupler 6N137 is used for isolation between the power circuit and control unit. The function of the driver circuit IR 2110 is utilized to amplify the pulses of the MOSFETs. The main features of the digital dsPIC30F4011 controller are listed as follows High-complexity FPGA integrated design environment, high Precision, Interchangeable textual, tabular, and graphical editors accelerate Rapid design visualization, analysis, and verification woven through the complete design flow Architecture aware implementation for all popular FPGA vendor families, Concurrent system integration with Mentor's PCB design processes to eliminate man weeks to months of error prone integration effort.

A. Line Variation



(a)



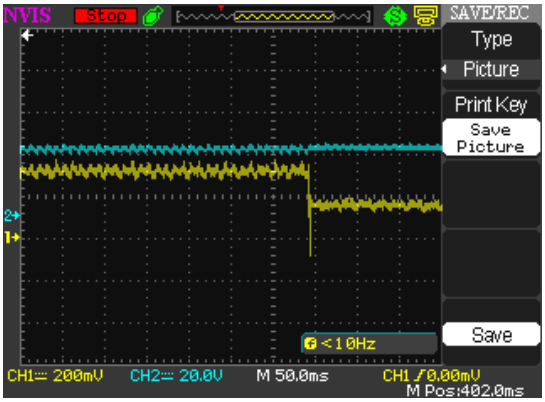
(b)

Fig.11 Experimental output voltage responses of the POESLLC using LQR plus FLC, (a) for input voltage step change from 12 V to 15 V, (b) input voltage step change from 15 V to 12 V [CH1: 20V/Div. output voltage; CH2:5V/Div. input voltage].

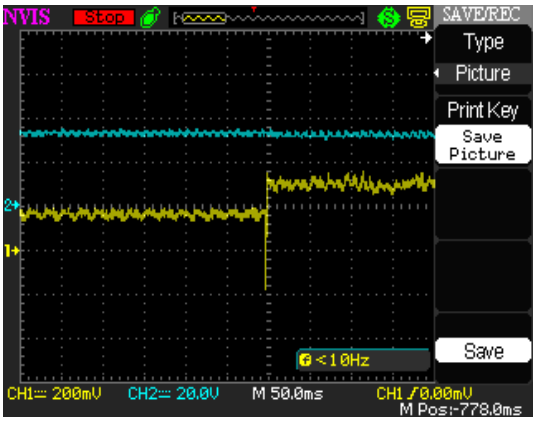
Fig.11 (a) Describe the experimental responses of the output voltage and input voltage of the POESLLC using the LQR plus FLC for input voltage step change from 12 V to 15 V. From this figure, it is clearly initiate that the experimental results of output voltage of the POESLLC with the designed LQR plus FLC has little overshoot and small settling time. Control algorithm can be implemented in FPGA digital platform.

Fig.11 (b) show the experimental responses of the output voltage and input voltage of the POESLLC using the LQR plus FLC for input voltage step change from 15V to 12V. It can be observed that the experimental responses of output voltage of the POESLLC using LQR plus FLC have minimal overshoot and zero settling time.

B. Load Variation



(a)



(b)

Fig.12 Experimental output voltage responses of POESLLC using LQR plus FLC, (a) for load change 40Ω to 60 Ω, (b) input voltage step change from load change 60Ω to 40Ω [CH1: 500mA/Div. output current; CH2:5V/Div. input voltage]

Fig. 12 (a) and (b) show the experimental results of output voltage and output current of the POESLLC with LQR plus FLC for load change 40Ω to 60 Ω and 60Ω to 40 Ω. It can be understood that the experimental results of output voltage of the POESLLC using designed controller has a little overshoot as well as fast settling time. Fig. 13 shows the experimental output voltage and inductor current of POESLLC using designed controller in steady state region. Fig. 14 indicates the experimental set-up model of the complete system. Also, the time domain analyses of the converter using controllers are listed in Tables 3 and 4. Finally, experiment and simulation results of POESLLC using designed LQR plus FLC has performed well in all the working conditions of the converter.

C. Steady state region

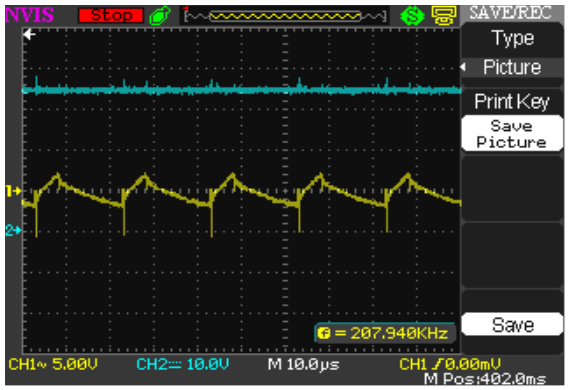


Fig. 13.Experimental result of output voltage and inductor current iL1 in steady state condition using PDIC plus FLC [Ch2:10V/Div - output voltage and Ch1:500mA/Div -inductor current].

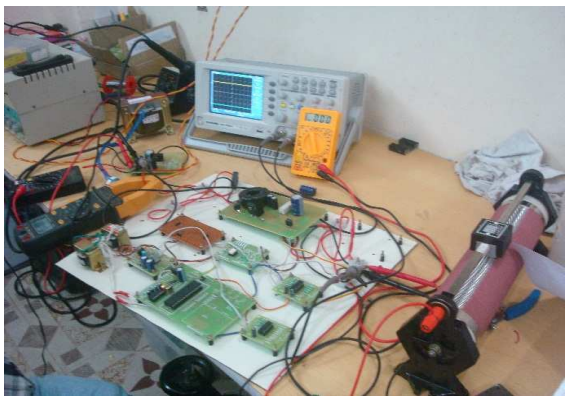


Fig 14. Experimental set-up of POESLLC using LQR plus FLC

6. CONCLUSIONS

The design and implementation of LQR plus FLC for POESLLC operated in CCM has been successfully established in MATLAB/Simulink as well as laboratory prototype models. The controller gains have been realized in digital FPGA. The simulation and experimental results are obtainable to exhibit the victory of the LQR plus FLC for the POESLLC worked in CCM resulted in excellent dynamic response, good load regulation, and output voltage of converter is not affected during the circuit component modifications, good steady state and magnificent transient responses. Therefore, it is more apt for any fixed power source real-world commercial applications, and it is essentially projected for power source in LED TV, mobile phones, and computer hardware.

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Table 3. Time Domain Analysis of the POESLLC using Controllers in Transient Region

Controllers	**LQR plus PDIC**	**LQR plus PDIC**	**LQR plus FLC**	**LQR plus FLC**
Results	**Experimental**	**Simulation**	**Experimental**	**Simulation**
Rise time(s)	0.05	0.03	0.06	0.02
Settling time(s)	0.08	0.05	0.03	0.02
Peak overshoot (%)	12	8	10	6
Steady state error	0	0	0	0
Output Ripple Voltage(V)	0.16	0.12	0.15	0.12

Table 4: Time domain Analysis of the POESLLC using Controllers

Results	**Controllers**	**Transient Region**		**Line variations**		**Load variations**	
		Maximum Overshoots (V)	**Settling Time (s)**	**Maximum Overshoots (V)**	**Settling Time (s)**	**Maximum Overshoots (V)**	**Settling Time (s)**
Simulation	LQR plus PDIC	0.45	0.0025	0.50	0.03	0.54	0.05
	LQR plus FLC	0.12	0.0018	0.12	0.01	0.13	0.03
Experimental	LQR plus PDIC	0.50	0.0035	0.54	0.05	0.56	0.07
	LQR plus FLC	0.16	0.0025	0.15	0.03	0.18	0.05