

IMPLEMENTATION OF 5-LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER WITH SINGLE DC SOURCE FOR PHOTO VOLTAIC SYSTEM USING PROTEUS

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Abstract

This paper begun with single phase 5-level Cascaded H-Bridge Multilevel (CHBML) inverter with transformer for Photo Voltaic system using PWM logical Switching technique. The input parameters voltage, current and the duty cycle D are used to generate the optimal MPPT under different operating conditions, The designed photovoltaic system which is simulated and constructed by photovoltaic array and a DC-DC buck converter. In MPPT technique the perturb and observe method is implemented. The major limitations of the cascade multilevel converters are requirement of Segregated DC voltage sources for Individual H-bridge which raise the converter expenditure and reduces the system reliability. This paper investigates different CHBM Inverter based topologies with reduced DC source by engaging low frequency transformers. The PWW Logical Switching technique is used with the help of gate circuit for Triggering MOSFET Switch in the CHBML Inverter.

Keywords: Photovoltaic system, Perturb & Observe Method, DC-DC Buck Converter, Cascaded H-Bridge Multilevel Inverter and Peripheral Interface Controller (PIC16F877A).

INTRODUCTION

Most of the natural resources such as wind, solar, geothermal, bio-gas, hydro are renewable and get replenished naturally. In this paper, implementation of Multilevel Inverter using MPPT based Perturb and Observe algorithm for PV cell is demonstrated. The Output of the system is not continuous due to the variation in the irradiance of solar energy because of the varying output voltage which lead to battery failure. In order to protect the battery from damage, a DC-DC Buck Converter with MPPT based P&O technique is connected in between solar module and battery. By using perturb and observe technique the switch conduction can be controlled which gives the constant voltage to the battery so that it can be protected [3].

In this project we are implementing the cascaded H-Bridge Inverter along individual DC Source and to reduced the Dc source the Cascaded H-Bridge are linked in parallel also to increases the output voltage level the low frequency transformer is utilized along with each Cascaded H Bridge Inverter. To trigger the

MOSFET switch in each cascaded H-Bridge inverter the logical gate circuit like OR,NOT, AND Gate signal are used .The use of logical operation is very much easy to implement for the closed loop operation of the system , so we can trigger the n number of switches like Multi level inverter.

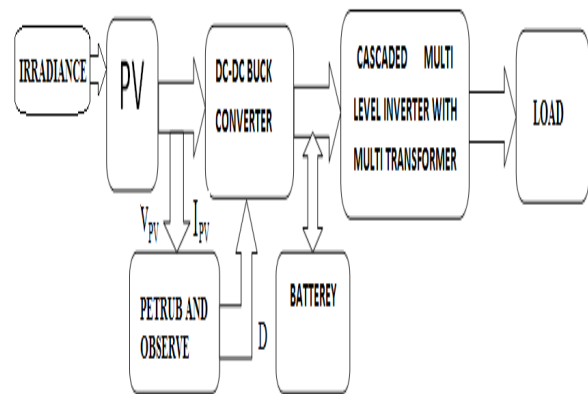


Figure 1 Block Diagram of PV Cell With CHBMLI

In this system the Proteus Software is used for real time application of implement the hardware circuit for Cascaded H-Bridge Multi Level Inverter. The PIC16F877A is used to generate the gate pulse for controlling for controlling the Mosfet switch in inverter.

PHOTO VOLTAIC MODULE:

The Solar cells are working under the condition of Photo Diode or Photo Voltaic Effect.

The Schematic diagram of Solar cell is shown in figure 2. The Solar cell consists of a DC source, Diode, parallel resistance R_{sh} and a series Resistance R_s .

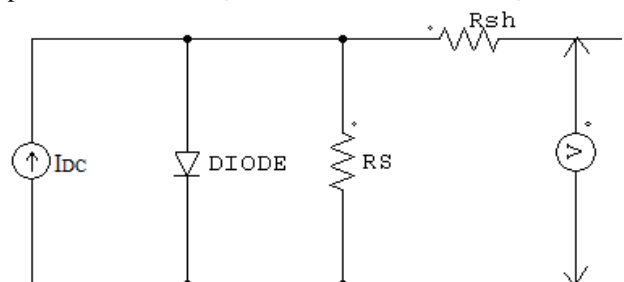


Figure 2 Circuit diagram of photo voltaic cell

A Photo Electric is arranged in the collection of varying photovoltaic cells in series and parallel network. In Series network are in charge for increasing the voltage of the module and when the parallel network is in charge of increasing the current in the array [4].

The output current from the photovoltaic array is

$$I = I_{SC} - I_d \quad (1)$$

$$I_D = I_o \left[\exp \left(\frac{U + IR_s}{\frac{nKT}{q}} \right) - 1 \right] \quad (2)$$

I_o =Reverse Saturation Current, n =Diode ideality factor , K =Boltzmann's Constant, T =Absolute Temperature & Q =Elementary Charge

$$I_D = I_o \left[\exp \left(\frac{U + IR_s}{\alpha} \right) - 1 \right] \quad (3)$$

$$I_L = \frac{\phi}{\phi_{ref}} \left[I_{Lref} + \mu_{ISC} (T_C - T_{Cref}) \right] \quad (4)$$

α =Thermal Voltage Timing Completion Factor , ϕ =Irradiance(W/m^2) , ϕ_{ref} = Reference Irradiance, I_{Lref} _Light current at reference condition, T_c _PV Cell Temperature, T_{cre} Reference Temperature & μ_{isc} -Temperature Coefficient of the short circuit current(A/C°)

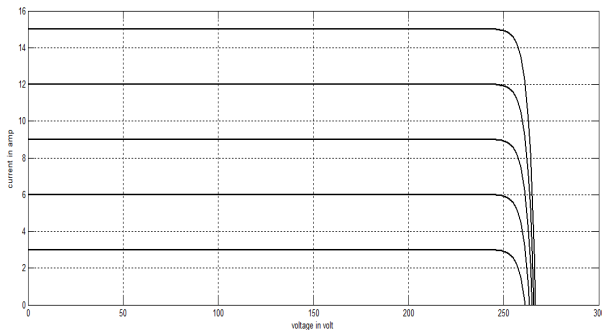


Figure 3 V-I Characteristics of Photovoltaic

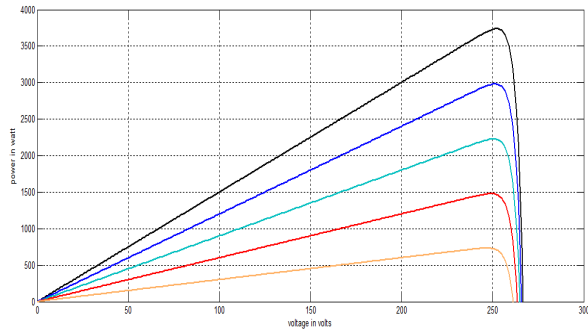


Figure 4 P-V characteristics curve of photovoltaic

Saturation Current I_o determination

$$I_o = I_{o,ref} \left(\frac{T_{C,ref} + 273}{T_c + 273} \right)^3 \exp \left[- \frac{E_{gap}}{kT_c} N_s \left(1 - \frac{T_{C,ref} + 273}{T_c + 273} \right) \right] \quad (5)$$

$I_{o,ref}$ = Saturation current at the reference condition in amp , E_{gap} =Band gap of the material

N_s =Number of cells in series of the PC

Module, q =Charge of the electron ($1.60217733 \times 10^{-19}C$)

α_{ref} =The value of α at the reference condition

$$I_{o,ref} = I_{L,ref} \exp \left(- \frac{U_{\alpha,ref}}{\alpha_{ref}} \right) \quad (6)$$

$U_{\alpha,ref}$ = The open circuit voltage of the PV Module at the reference condition (v)

MAXIMUM POWER POINT TECHNIQUE

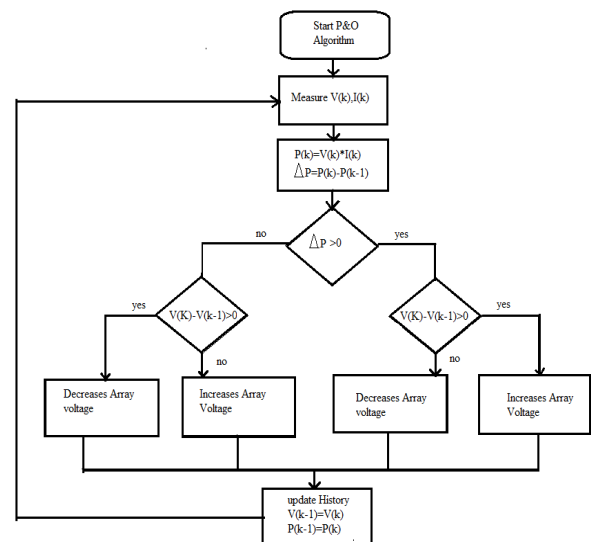
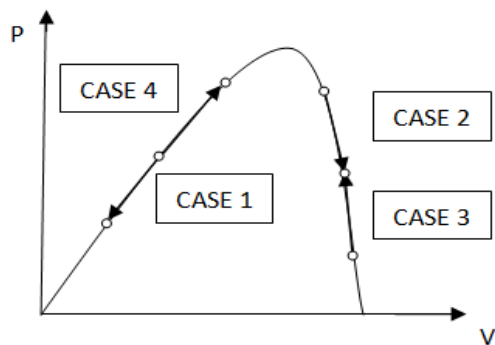


Figure 5 flow chart of perturb and observe algorithm

In Photo voltaic cell the output voltage will be 30 to 40 percent. To raise the voltage of the photo voltaic cell the Maximum power point tracking is implemented. MPP keeps changing during day-time and need for tracking MPP time to time. This helps the panel to yield maximum power throughout the operation. From the V-I characteristics, MPP is identified by examining the point where both the current and voltage are at their maximum. If connected directly to the load, the MPP will be at the crossing of I-V characteristics of PV panel and the IV-characteristics of the load. This derived crossing point is not the original PV array's maximum power point. The PV's crossing point is held at the MPP by regulating the voltage and current of PV array independently with regard to the load using switch-mode power converter[4].



CASE	dp	dv	Action
1	<0	<0	+
2	<0	>0	-
3	>0	<0	-
4	>0	>0	+

Figure 6 P-V Characteristics of Solar panel.

The most widely accepted MPP method is Perturb & Observe due to its ease of implementation and low cost. This may result in top level efficiency, with the criteria that a proper predictive and adaptive hill climbing strategy is acquired. Voltage and current of the PV panel should be measured continuously. Power is computed by finding the product of current and voltage. Foremost, the difference in power of existing with the previous power should be calculated and also the difference in the voltage of two successive intervals should be found. Depending on this power difference and voltage difference the four cases are to be studied as follows [9].

First two cases occur when $\Delta P > 0$ where $\Delta P = P_k - P_{k-1}$
 Case 1: $\Delta P > 0$ and $V_k - V_{k-1} > 0$ (7)

If we infer from this that PV array's operating voltage is perturbed in the given direction and the power obtained from the PV array is enhanced, the operating point also has shifted towards the MPP and hence the perturbation of the operating voltage should be continued in the same direction.

Case 2: $\Delta P < 0$ and $V_k - V_{k-1} > 0$ (8)

Decrease the voltage

Case 3: $\Delta P > 0$ and $V_k - V_{k-1} < 0$ (9)

Here, when the power increases and the voltage decreases compared to the previous voltage, then the perturbation of voltage should be reversed (i.e.) decrease in the voltage. In the cases where $\Delta P < 0$, the power drawn is decreased and the operating point is drifted abroad from the MPP.

Case 4: $\Delta P < 0$ and $V_k - V_{k-1} < 0$ (10)

When the power decrease and voltage decrease, the perturbation of voltage is increased.

CASCADE H-BRIDGE

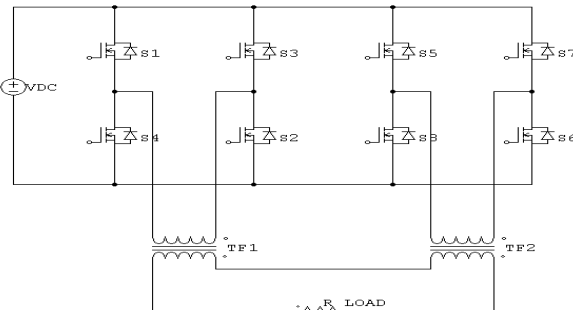


Figure 7 CHBMLI with low frequency transformer

A Five level CHBMLI with one Dc source using transformer as shown in figure 7 Normally the n no of CHBML inverter are connected in series to increases the n no of levels. The main drawbacks of this system are it requires a single Dc source for each Cascaded H bridge (CHB) inverter. To reduce the no of DC source and to maintain with single Dc source for CHB inverter are connected in parallel. Here we are using two CHB Inverter are connected in parallel connection and the output of each CHB inverter the primary side of the transformer is linked in parallel. The secondary side of two transformer are connected in series with Resistive load. The output voltage level for two cascaded H bridge inverter is $+2V_{dc}, +V_{dc}, 0V, -V_{dc}$ & $-2V_{dc}$ [3].

Logical Switching Circuits

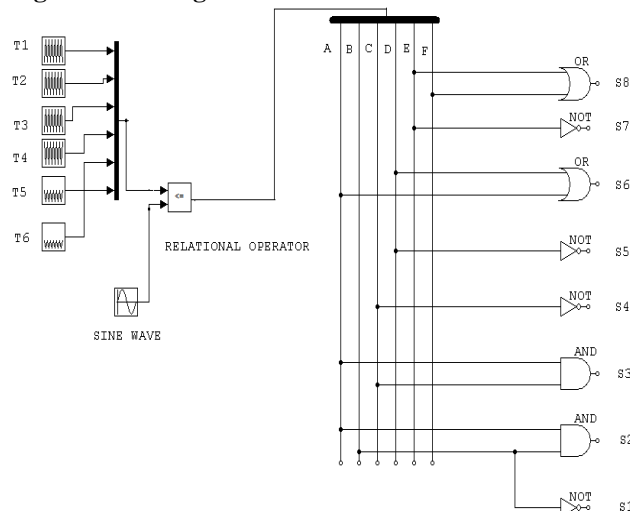


Figure 8 switching logical function for 5-level CHBML Inverter

The switching logical function of 5-level CHBML inverter as shown in figure 8. The step by step triangular wave is generated from 1 to -1 v with switching frequency of 2khz. The sine wave and triangular wave is compared with relation operator to generate PWM signal. Using logic gate like AND, OR and NOR is compared

to generate the shifted PWM for switches as shown in Table I.

TABLE I. SWITCHING LOGICAL CIRCUITS

Pulse	Logical operation
S_1	\overline{B}
S_2	$A+B$
S_3	$A+C$
S_4	\overline{C}
S_5	\overline{D}
S_6	$D+A$
S_7	\overline{E}
S_8	$E+F$

SIMULATION

The Figure 9 display the simulation of Buck converter (BC) with 5-Level CHBML Inverter. The Solar panel is designed with Open circuit voltage of 88.8v and short circuit current of 4.5A as shown in figure 10 with different irradiance .The output of solar panel is connected with Buck Converter .In Buck Converter the MOSFET switch is controlled by petrub and observe technique. The output of Buck Converter is connected to 5-Level inverter and the primary side of the transformer are connected parallel to the output of each H-Bridge inverter [5].

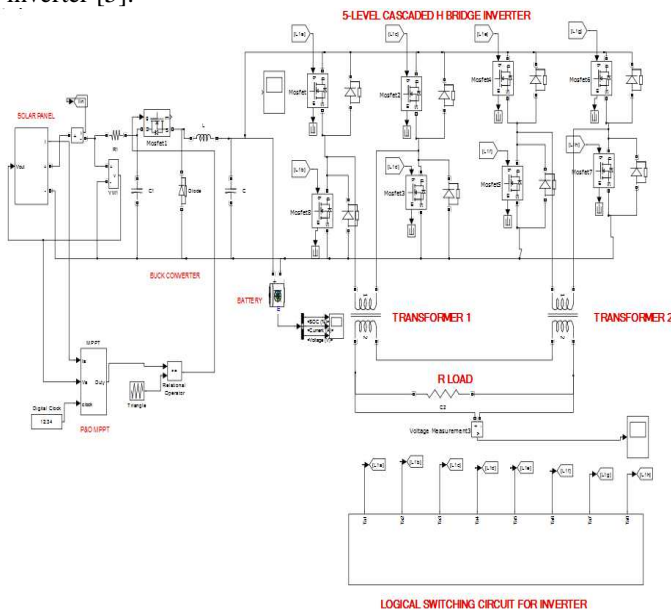


Figure 9 Simulation of Buck Converter with 5level CHBMLI

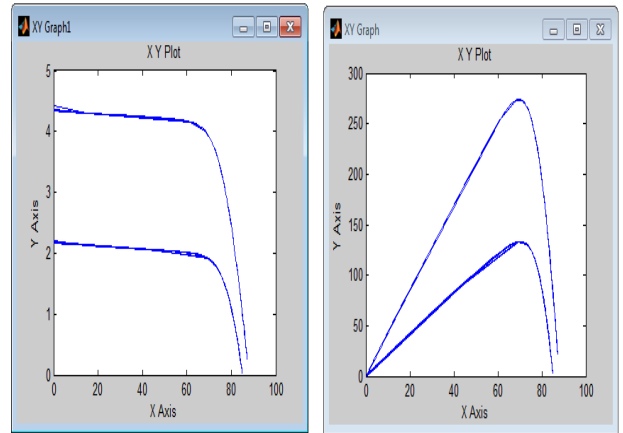


Figure 10 V-I & P-V Characteristics of solar panel

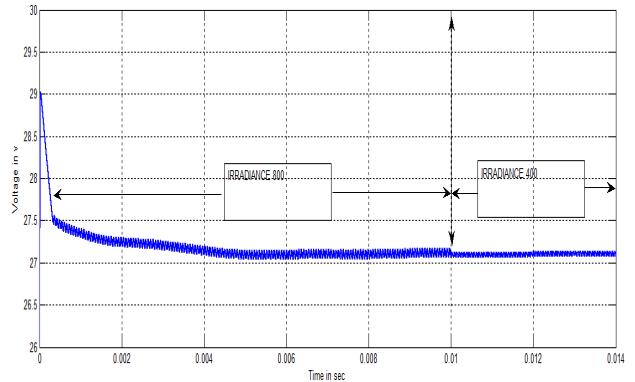


Figure 11 Buck Converter output Voltage.

The figure 11 shows the Buck Converter output voltage. The input voltage is 88.8v and output voltage is 27v. When the irradiance is changes from 800 to 400 the Buck Converter output voltage is maintain as constant .

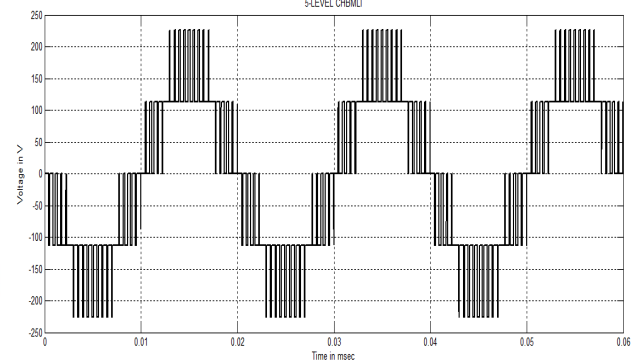


Figure 12. Five level CHBMLI Inverter with PWM Logical switching control .

The figure 12 Shows the Five level CHBMLI inverter with transformer. The input for inverter is 27v and the output voltage is 240v and it is increased by transformer .The voltage levels are 240v,120v, 0v,-120v,-240v respectively. The Logical switching technique is used to control the Mofset switch and to reduce the THD (Total Harmonic Distortion) in the Inverter [7].

HARDWARE IMPLEMENTATION

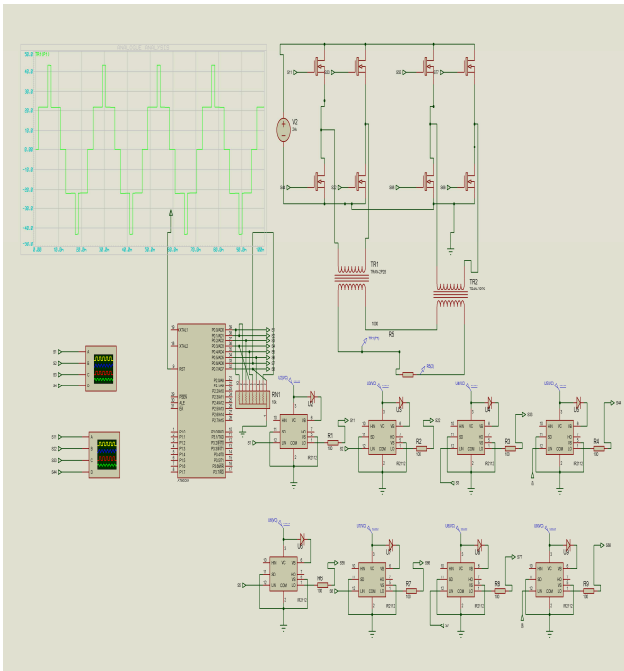


Figure 13 Proteus Design for 5-Level CHBML Inverter

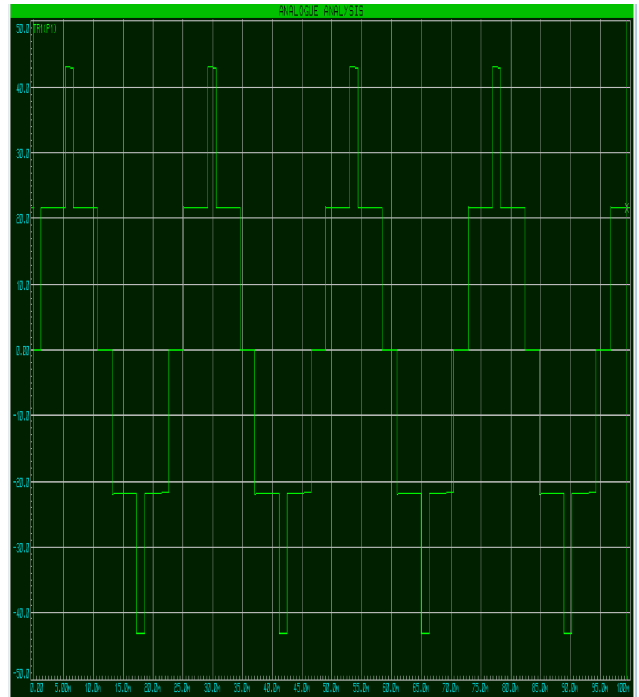


Figure 14 Output Voltage for 5-Level CHBML Inverter

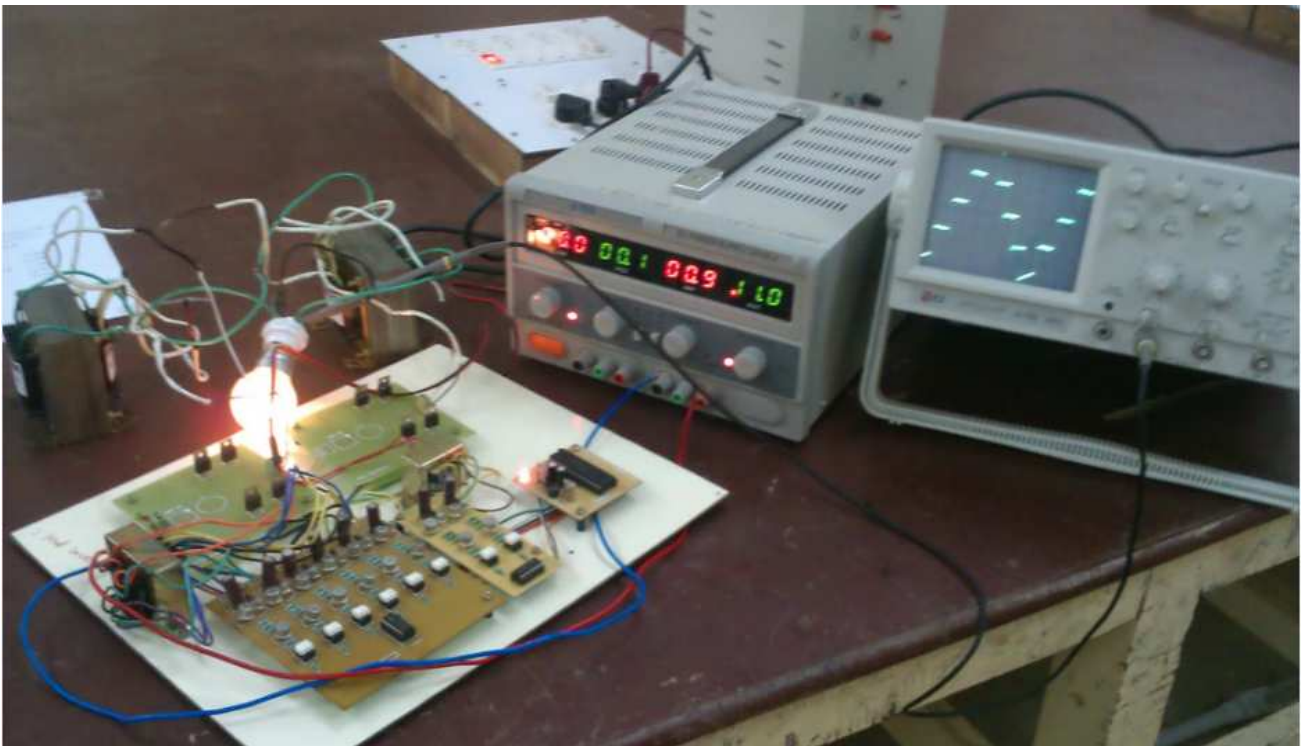


Figure 15 Hardware implementation of five level CHBML Inverter

The PIC16F877A is used for generating required gate pulse of 5 volt. This 5 volt gate is boosted to 11 V by using International Rectifier (IR2112). The output of IR2112 is driven to Mosfet switch IRF640. It has high voltage and current carrying capability are shown in figure 13 by using Proteus Software.

In Hardware circuit the Transformer primary voltage rating (0v,9v,10v,11v,12v) and secondary voltage rating is 110v.. The input voltage for inverter is 9v and output voltage is 110v. The output voltage of 5level inverter in Proteus software and Hardware circuit as shown in figure 14 and 15.

The figure 16 show the output voltage of inverter is 110V and load current is 0.15A .The output power rating is 16.5W. The THD is analyses for n number of harmonics for 5-level cascaded h bridge inverter as shown in figure 17.

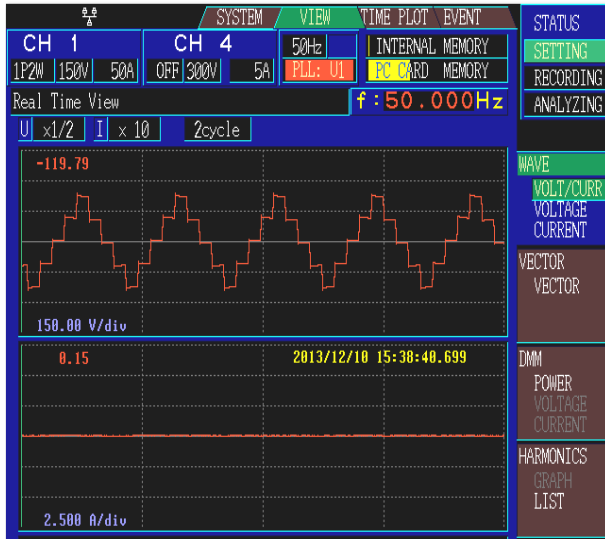


Figure 16 Output Voltage and Current for five level CHBMLI



Figure 17 THD Analysis for 5-Level inverter.

CONCLUSION

In this paper the photo voltaic system with MPPT based perturb and observe algorithm are utilized by using embedded Matlab file. The output of Duty cycle is controlling the MOSFET switch in DC-DC Buck Converter. The MPPT can be enriched by minimizing the oscillation of the operating point around the maximum power in steady state and dynamic output. The CHBMLI is connected with a single Dc source and transformer is to increases the output voltage level. The switching sequence

for MOSFET is designed by using logical gate circuit .The proteus software and hardware is implemented for 5-level inverter circuit by using PICF877A Controler.

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