Single-Phase SOGI-PLL Based Reference Current Extraction for Three-Phase Four-Wire DSTATCOM

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Abstract— This paper describes a novel control algorithm based on single-phase SOGI (Second Order Generalized Integrator) PLL (Phase Locked Loop) for a three-phase four-wire DSTATCOM (Distribution Static Compensator). The proposed DSTATCOM performs various functions such as load balancing, harmonic mitigation, reactive power compensation and neutral current compensation under distorted load conditions. This control algorithm extracts the fundamental component of the load currents for estimating the reference currents based on three single-phase SOGI-PLLs. The main objective of the controller is to reduce the overall complexity and computational burden. SOGI-PLL is enhancing the capability of reference current tracking for compensation under the step changes in load currents. During the design procedure, the effects of load unbalancing and sudden increase/decrease in loads are also taken into account and performance is found satisfactory. The effectiveness of the design is simulated and shown using MATLAB/Simulink.

Index Terms— Second Order Generalized Integrator, Phase -Locked Loop, DSTATCOM, Load balancing, Power Quality (PQ).

I. INTRODUCTION

EFFICIENT phase tracking capability for utility grid voltage is the important factor in converters for custom power applications. The reference component generated from the phase-locked loop decides the performance of the converters for compensating power quality problems such as load unbalance, harmonic mitigation, high neutral current and reactive power compensation. The PLL should respond effectively in distorted load conditions by detecting the phase angle and amplitude at a faster rate. In recent days, Non-linear loads are increased extensively at the utility end and causing power quality problems at the PCC in the supply system [1].

These nonlinear loads include diode bridge rectifiers, variable speed drives, thyristor converters and variable power supplies [3]. Harmonics play a major role in the power quality problems at the consumer end and shunt active power filter is the crucial tool in mitigating harmonics and also other PQ issues [2] [4]. Various researchers have discussed numerous control techniques for estimation of reference components to mitigate PQ problems using a three-phase four-wire DSTATCOM. The neutral current should not be more than 20% of the full load current [5]-[6]. Several PLL techniques have been introduced for detecting the amplitude and phase angle for grid-connected systems. A three phase Synchronous Reference Frame PLL gives satisfactory performance under ideal conditions but poor performance under distortion [7]. The DFT (Digital Fourier Transform) and RDFT (Recursive Digital Fourier Transform) are frequency domain approaches that suffer from high computational burden but widely used owing to accuracy [8]-[10]. Josep M. Guerrero and Saeed Golestan have been deeply analyzed the structures of two different PLLs namely SOGI and Park PLL [11]. The LPN-PLL and Pre-filtered SRF PLL was excellent under steady-state and

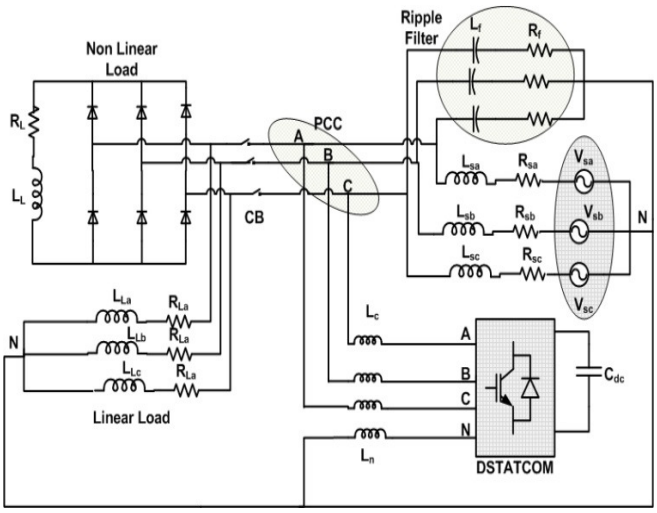


Fig. 1 Line Diagram of the Proposed System.

transient conditions in comparison with SRF-PLL [12]-[13]. Several control algorithms has been developed for the satisfactory operation of DSTATCOM [14]-[16].

In this paper, a novel control algorithm using SOGI-PLL has been introduced for extracting the reference components under distorted load conditions. The proposed algorithm maintains balanced sinusoidal currents with stiff DC bus voltage at DSTATCOM. This control algorithm is used to reduce harmonics and reactive power compensation under unbalanced non linear loads. The control structure has advantages, a) Amplitude and Phase detection according to the change in requirements. b) Speed and Accuracy c) fundamental component extraction under adverse load conditions. Finally, an effective implementation of the algorithm to reduce the overall computational burden, low bulkiness and low complexity in design and variable compensation for three-phase four-wire DSTATCOM is presented. This approach is based on single-phase SOGI-PLL to extract three phase reference components. In this technique, Power quality improvement with neutral current compensation is also done using a four leg VSC and the effectiveness of the system is shown through simulation results. Simulations are carried out using MATLAB/Simulink, simpower systems block set.

II. PROPOSED SYSTEM CONFIGURATION

Fig. 1 shows a line diagram of the proposed system with control diagram for a four leg VSC (Voltage Source Converter) feeding nonlinear loads. The DSTATCOM is connected in parallel to the source and load at the Point of Common Coupling (PCC) through interfacing inductor L_c to reduce the ripple currents in the controller current. The VSI based DSTATCOM is capable of suppressing the harmonics in the source currents, power factor correction and load balancing. A small capacity rated R-C filter is connected in parallel with the source to eliminate the high switching ripple content of the VSC. DSTATCOM is connected to the a.c mains through source impedance (R_s, L_s) and Loads. The load under consideration is a combination of linear and non-linear type. A ripple filter (R_f, C_f) is also connected in parallel to the load and source to reduce the high frequency noise at the PCC. The controller currents (I_{ca}, I_{cb}, I_{cc}) are injected into PCC to compensate harmonics and reactive power in the load. The load current is sensed and made as input to the SOGI PLL to extract the accurate phase and amplitude. The SOGI PLL is chosen because of its low computational burden and desired performance under distorted conditions.

III. CONTROL ALGORITHM

The control algorithm consists of four modules: SOGI PLL, Active & Reactive Component Extraction, Reference Current Generation and Current Controller.

A. *SOGI-PLL*

The basic block diagram of the PLL is shown in Fig.2. The basic PLL consists of three building blocks as shown in Fig.2. 1) Phase Detector that generates a signal which is the difference in phase between the input and feedback signal and then it is passed through the loop filter (LF). 2) LF is used to control the Voltage Controlled Oscillator (VCO). 3) VCO generates the frequency signal from its nominal frequency.

The proposed method of designing a SOGI PLL is shown in Fig. 3. In fig (3b), the outputs $I_{L\alpha}$ and $I_{L\beta}$ generates two sine waves with a phase shift of 90^0. The component $I_{L\alpha}$ and I_L has the same magnitude and phase. The SOGI structure is defined as [11].

$$GI = \frac{w}{s^2 + w^2} \tag{1}$$

Where w- Resonance Frequency of the SOGI

$$H_d = \frac{I_{L\alpha}}{I_L} \tag{2}$$

$$H_q = \frac{I_{L\beta}}{I_L} \tag{3}$$

The k shown in figure.3 affects the bandwidth of the closed-loop system. When the grid frequency has fluctuations, problems may occur as the structure is frequency dependent. Hence, the w value of the SOGI is tuned according to the frequency provided by the PLL structure.

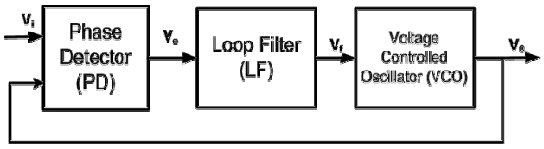


Fig. 2 Block Diagram of PLL.

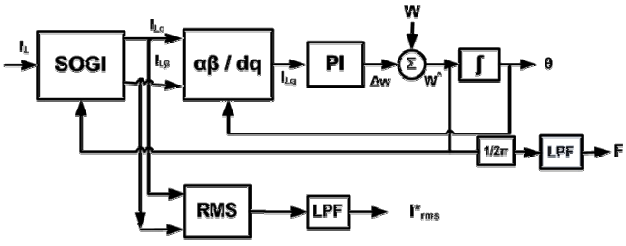
Using the proposed method, the input I_L if filtered leading to two waveforms ($I_{L\alpha}$ and $I_{L\beta}$) because of the resonant frequency. The gain *k* decides the level of filtering and the filter band pass becomes narrower and dynamic response will become slower with the decrease in *k*. Park transformation is used to convert αβ to dq.

$$T = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \quad (4)$$

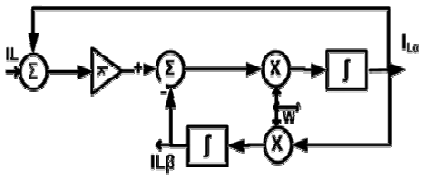
To attenuate the high frequency noises, the transformation output I_{Lq} is passed through a Proportional – Integral (PI) controller. The fundamental frequency (W_{ff}) is added to the PI control signal and then it is integrated to generate the estimated phase angle $\hat{\theta}$. In order to get a balanced set of in-quadrature outputs with exact amplitudes, the SOGI frequency must be equal to the input fundamental frequency.

B. Estimation of Unit Voltage Templates

The basic equations for estimation of the different control signals are shown below. The three phase source voltages may be unbalanced or consists of harmonics and those are processed through filters to eliminate the noise and harmonics. The individual phases are estimated through squaring them and then processed through filters as follows [16].



(a)



(b)

Fig. 3 a) Basic Design of SOGI PLL b) SOGI Block .

$$V'_{ta} = \sqrt{\left[2\left(\frac{v^2_{sa}}{2}\right)\right]}, \quad (5)$$

$$V'_{tb} = \sqrt{\left[2\left(\frac{v^2_{sb}}{2}\right)\right]} \quad (6)$$

$$V'_{tc} = \sqrt{\left[2\left(\frac{v^2_{sc}}{2}\right)\right]} \quad (7)$$

Where, (v_{sa}, v_{sb}, and v_{sc}) are the phase voltages and V_{ta}', V_{tb}', V_{tc}' are the constant value amplitudes.

The In-phase unit templates of PCC voltages are estimated as:

$$u_a = \frac{v_{sa}}{V_{ta}}; u_b = \frac{v_{sb}}{V_{tb}}; u_c = \frac{v_{sc}}{V_{tc}} \quad (8)$$

Quadrature unit templates of PCC voltages are estimated as:

$$w_a = \frac{(-u_b + u_c)}{\sqrt{3}}, w_b = \frac{(3u_a + u_b - u_c)}{2\sqrt{3}}, \quad w_c = \frac{(-3u_a + u_b - u_c)}{2\sqrt{3}} \quad (9)$$

The amplitude of the PCC voltage is estimated as:

$$v'_t = \sqrt{\frac{2\left(v^2_{sa} + v^2_{sb} + v^2_{sc}\right)}{3}} \quad (10)$$

This amplitude (v'_t) is supplied to the low pass filter to reduce the ripples and to attain the amplitude of the fundamental positive-sequence voltages for controlling the PCC voltages. These unit vector templates are now used to extract the active and reactive components of currents.

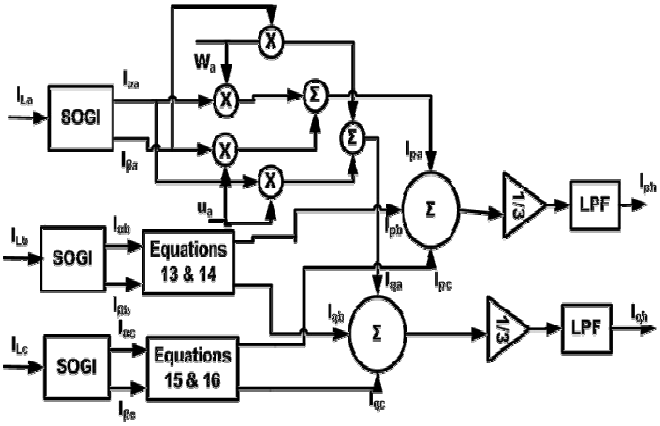


Fig.4 Block Diagram of Active and Reactive Component Extraction

C. Active and Reactive Component Extraction

Fig.4 shows the block diagram of the active and reactive component extraction based on SOGI PLL scheme. In this algorithm, load currents (I_{La}, I_{Lb}, I_{Lc}), unit vector (u_a,u_b,u_c)

and quadrature vector templates (w_a,w_b,w_c) are required for extraction of in-phase (I_{ph}) and quadrature currents (I_{qh}).

The in-phase component and quadrature component for each phases a,b,c are calculated as follows:

$$i_{pa} = i_{\alpha a} w_a + i_{\beta a} u_a \quad (11)$$

$$i_{qa} = -i_{\alpha a} u_a + i_{\beta a} w_a \quad (12)$$

$$i_{pb} = i_{\alpha b} w_b + i_{\beta b} u_b \quad (13)$$

$$i_{qb} = -i_{\alpha b} u_b + i_{\beta b} w_b \quad (14)$$

$$i_{pc} = i_{\alpha c} w_c + i_{\beta c} u_c \quad (15)$$

$$i_{qc} = -i_{\alpha c} u_c + i_{\beta c} w_c \quad (16)$$

The average amplitude of active and reactive components of the three phase load currents are estimated for load balancing and to be used in the extraction of three phase source currents as:

$$i_{ph} = \frac{i_{pa} + i_{pb} + i_{pc}}{3} \quad (17)$$

$$i_{qh} = \frac{i_{qa} + i_{qb} + i_{qc}}{3} \quad (18)$$

D. Reference Current Generation

Fig.5 shows the block diagram of the reference current generation. This block requires DC link voltage (V_{dc}), Load Voltages (V_{abcL}), active, reactive component of currents (I_{ph}, I_{qh}) and unit vector templates to generate the reference source currents.

The voltage across the DC capacitor V_{dc} is sensed and compared with the reference DC bus voltage V^*_{dc} and this error at the n^{th} sampling instant is expressed as:

$$V_{de}(n) = V^*_{dc}(n) - V_{dc}(n) \quad (19)$$

This voltage error is fed to PI controller to maintain the DC voltage of the DSTATCOM. At n^{th} sampling instant, the output of the PI controller is as:

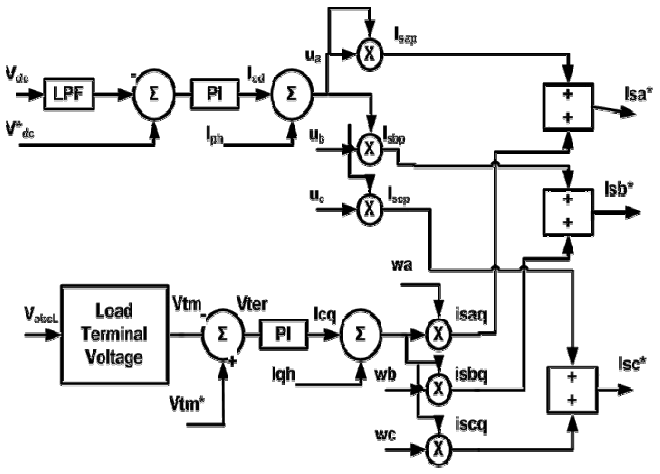


Fig.5 Block Diagram of Reference Currents Generation

$$I_{cd}(n) = I_{cd}(n-1) + k_{pt}\{v_{dcer}(n) - v_{dcer}(n-1)\} + k_{it} v_{dcer}(n) \quad (20)$$

Where, K_{pt} and K_{it} are the proportional and integral gain constants of the PI controller. $V_{de}(n)$ and $V_{de}(n-1)$ are the voltage errors of the DC bus in n^{th} and $n\text{-}1^{th}$ instant and $I_{cd}(n)$ and $I_{cd}(n-1)$ are the amplitude of active power component of the fundamental reference current at n^{th} and $(n-1)^{th}$ instant.

$$i_{sap} = u_a \left(I_{ph} + I_{cd} \right) \quad (21)$$

$$i_{sbp} = u_b \left(I_{ph} + I_{cd} \right) \quad (22)$$

$$i_{scp} = u_c \left(I_{ph} + I_{cd} \right) \quad (23)$$

The output of the PI controller (I_{cd}) is summed to the amplitude of active component (I_{ph}) and the resultant is multiplied with the unit vector of the three phases (u_a, u_b, u_c) to generate the amplitude of fundamental active component of current I_{sap}, I_{sbp} and I_{scp} respectively as shown in fig.5.

The voltage across the load is used to generate the amplitude of the load voltage (V_{tm}) as in (10) and compared with the reference load voltage V^*_{tm} and this error at the n^{th} sampling instant is expressed as:

$$V_{ter}(r) = V_t^*(r) - V_t(r) \quad (24)$$

This voltage error is fed to PI controller to regulate the AC voltage to its reference value. At n^{th} sampling instant, the output of the PI controller is as:

$$I_{cq}(r) = I_{cq}(r-1) + k_{pt}\{V_{ter}(r) - V_{ter}(r-1)\} + k_{it} V_{ter}(r) \quad (25)$$

Where, K_{pt} and K_{it} are the proportional and integral gain constants of the PI controller. $V_{ter}(r)$ and $V_{ter}(r-1)$ are the voltage errors of the AC bus in r^{th} and $r\text{-}1^{th}$ instant and $I_{cq}(r)$ and $I_{cq}(r-1)$ are the amplitude of reactive power component of the fundamental reference current at r^{th} and $(r-1)^{th}$ instant. The output of the PI controller (I_{cq}) is summed to the amplitude of reactive component (I_{qh}) and the resultant is multiplied with the unit quadrature vector of the three phases (w_a, w_b, w_c) to generate the amplitude of fundamental reactive component of current I_{saq}, I_{sbq} and I_{scq} respectively as shown in fig.5.

$$i_{saq} = w_a \left(I_{qh} + I_{cq} \right) \quad (26)$$

$$i_{sbq} = w_b \left(I_{qh} + I_{cq} \right) \quad (27)$$

$$i_{scq} = w_c \left(I_{qh} + I_{cq} \right) \quad (28)$$

Finally, the active and reactive component of currents are summed to generate reference supply currents I_{sa}*, I_{sb}*, I_{sc}* respectively.

$$i^*_{sa} = i_{sap} + i_{saq} \quad (29)$$

$$i^*_{sb} = i_{sbp} + i_{scq} \quad (30)$$

$$i^*_{sc} = i_{scp} + i_{scq} \quad (31)$$

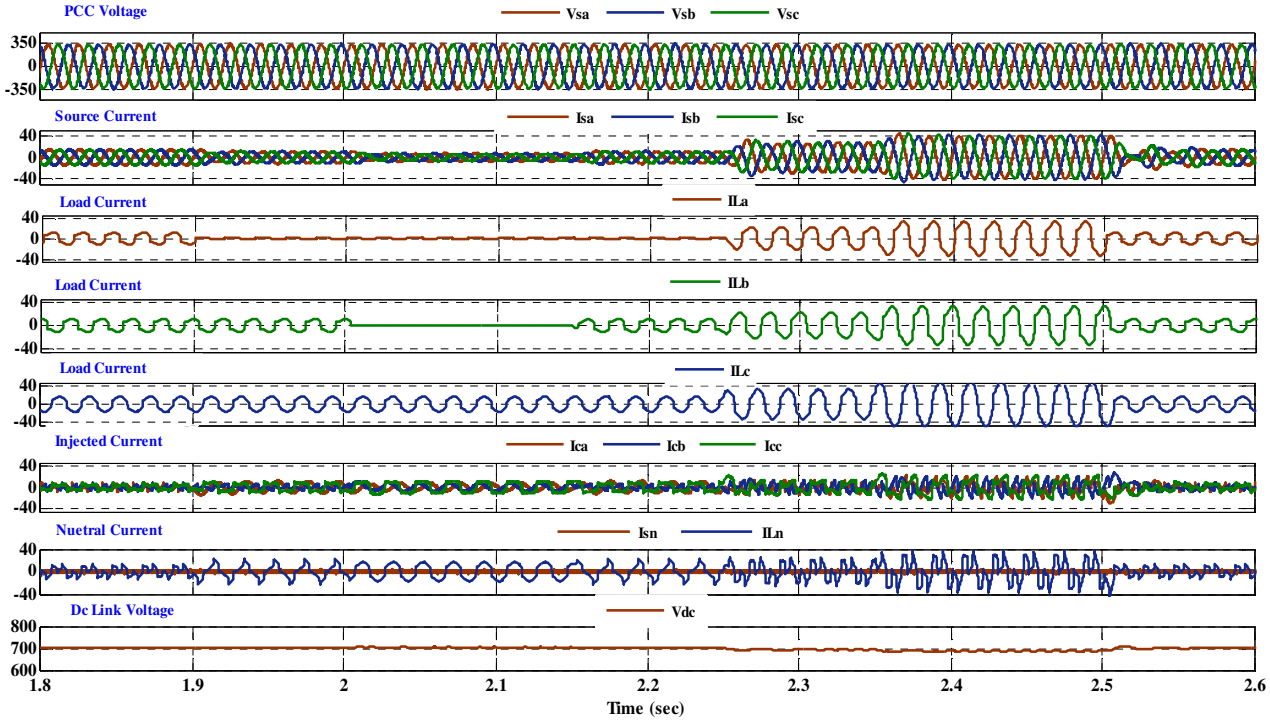


Fig. 6 Performance of DSTATCOM for the considered

These estimated three phase reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) and i^*_{sn} are compared with sensed source currents (i_{sa}, i_{sb}, i_{sc}) and i_{sn} ($i_{sa}+i_{sb}+i_{sc}$) to estimate the current errors. These errors are regulated using PI controllers and are compared with carrier signals to generate PWM pulses for DSTATCOM.

IV. Simulation Results and Discussion

The proposed control algorithm for three-phase four-wire DSTATCOM is modeled in MATLAB / Simulink using Simpower systems toolbox. The performance of the control algorithm is studied for harmonic compensation, load compensation/neutral current Compensation and Power Factor correction/Reactive Power Compensation which are discussed individually in this section. Fig. 6. Shows the PCC-Voltage (Vpcc), Source Current (Is_abc), Load Currents – (I_{La},I_{Lb},I_{Lc}), Compensation Currents (Ic_abc), Neutral Currents (I_{N_S},I_{N_L}) and the DC-Bus voltage (Vdc). The parameters for the system are given in appendix.

A. *Harmonic Compensation*

Fig. 7 and Fig.8 shows the results for the case harmonic compensation. A single phase-current source type of nonlinear load is applied on all the three phases for which the source currents are obtained sinusoidal. The harmonic spectrum for the nonlinear load currents and the obtained source currents are shown in the fig. 8. Load current (I_{La}) have a THD of 25.17% with a fundamental component of 35.44A and the source current has a THD of 1.73% with a fundamental component of 40.19A. Thus, the magnitude and THD of the Load currents and the source currents shows the effectiveness of the proposed control algorithm.

B. *Load / Neutral Current Compensation*

The performance of the DSTATCOM with the proposed control algorithm for the unbalanced and varying loads for the case of load compensation/neutral current compensation is shown in fig.7 and fig.10. The unbalance in the load is created by opening the phase ‘a’, phase ‘b’ during 1.9sec to 2.25sec and 2sec to 2.15sec respectively.

Table-I

Quantity	Load Currents	Source Currents	Load Currents	Source Currents	Load Currents	Source Currents
	THD %	THD %	THD %	THD %	THD %	THD %
	Normal Condition		Un-Balanced Condition		Increase in Load Condition	
Ph-a	25.17	1.73	64.28	4.73	20.12	1.65
Ph-b	25.15	1.77	66.12	4.98	20.18	1.69
Ph-c	16.58	1.77	17.29	3.56	18.23	1.71

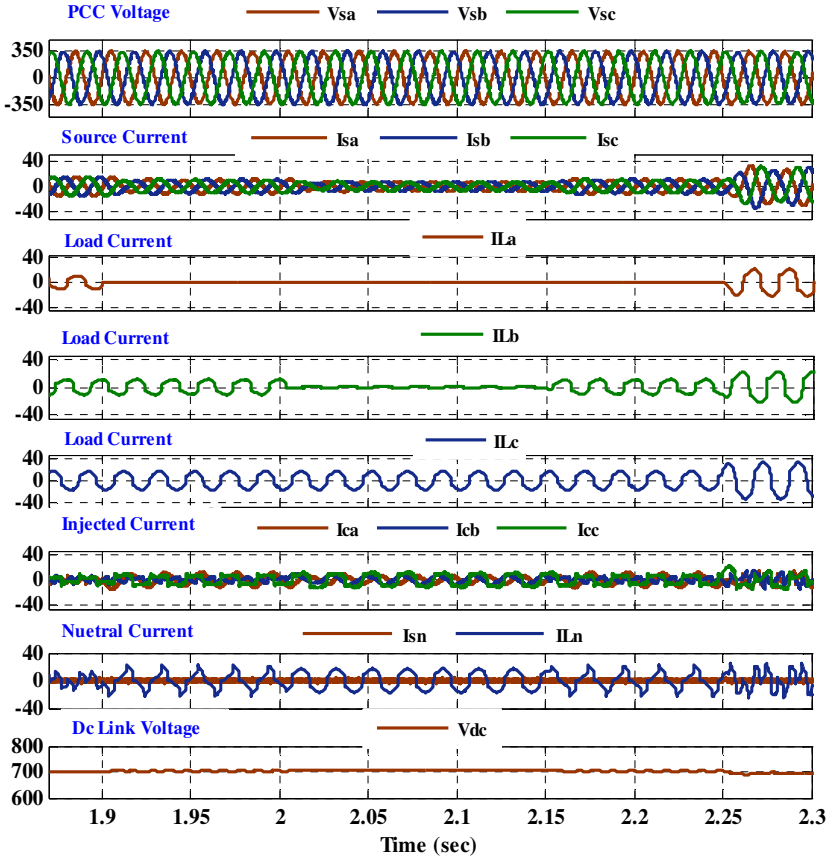


Fig. 7 Performance of DSTATCOM under unbalanced and varying nonlinear loads

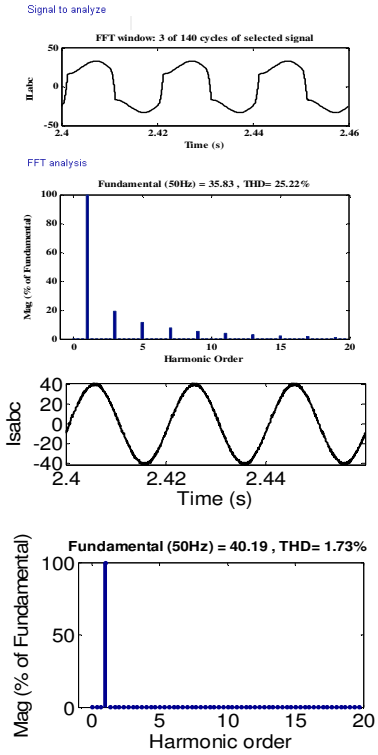


Fig. 8. Harmonic Spectrum of 'a'-ph of Load Current and Source Current

The increase in load neutral current can be observed with the increase in the unbalanced load currents shown in fig.10. The source neutral current is observed to be almost zero, which presents the effectiveness of the control algorithm. The source currents are observed to be balance under all these conditions. The DC bus voltage of DSTATCOM is regulated to the reference value under all load conditions. The values of each phase currents are tabulated with all the conditions in Table-I.

C. Reactive Power Compensation / Power Factor Correction

Power factor correction at various load conditions are shown in Fig. 9. The source voltage is scaled to (1/20)V for effective visualization of zero crossing of source current (I_{sa}) and Source Voltage (V_{sa}). From the figure, it can be observed that the source current is in phase with the source voltage at various load conditions.

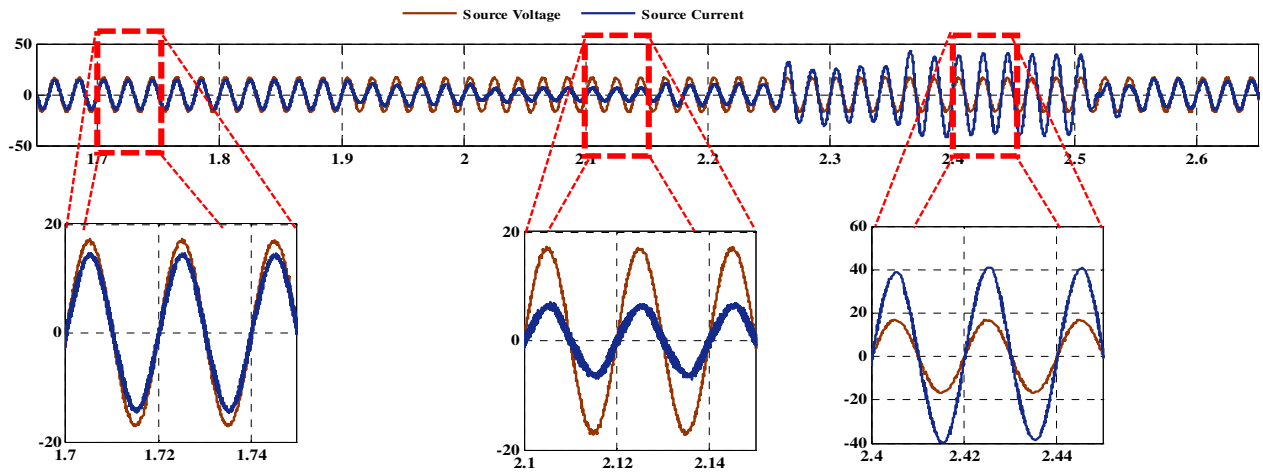


Fig. 9 Results presenting the zero crossing of source voltage and source current at various load levels

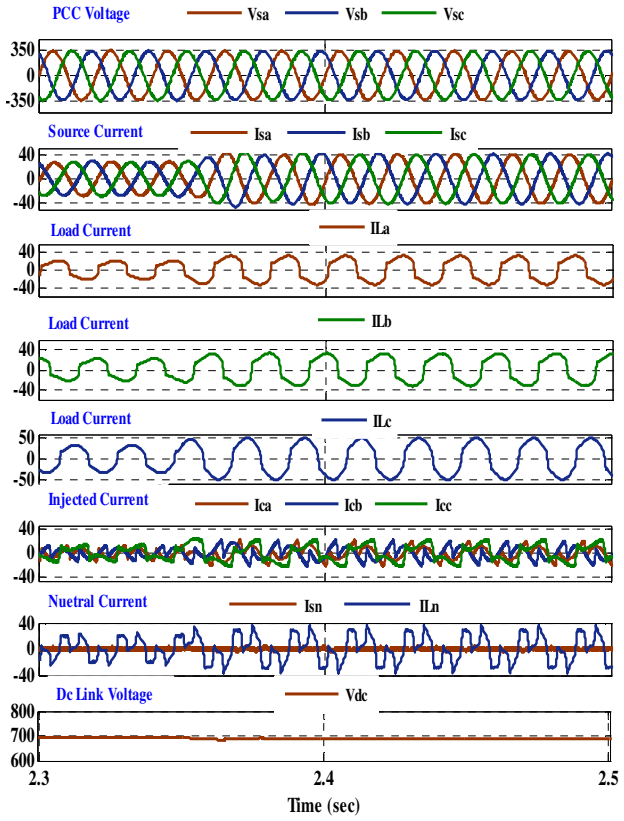


Fig.10 Performance of DSTATCOM under Varying Nonlinear load conditions

A three-leg single-phase voltage source converter (VSC) based DSTATCOM [15] requires 12 switches and hence the cost and complexity is high. The split capacitor based VSC has a disadvantage of maintaining same DC voltage at the series capacitors [15]. Zig-Zag transformer with three-leg VSC has better performance in neutral current compensation but costly and effective design should be done [16]. A T-connected transformer also requires two single-phase transformers and compensation has no much change compared with the zig-zag transformer [17]. A star/delta transformer is also reported in the literature for neutral current compensation [18]-[20]. The disadvantages of the above mentioned topologies require an additional transformer specially designed for proper compensation. Because, the level of compensation is affected by the transformer impedance. The four-leg VSC based DSTATCOM is superior and requires 8 switches but the controller is to be tuned accordingly. The proposed controller has proved its effectiveness in voltage regulation, harmonic elimination, power factor correction, neutral current compensation and load balancing.

V. CONCLUSION

A control algorithm based on SOGI-PLL for DSTATCOM has been implemented for compensation of three-phase four-wire non-linear - Unbalanced and Varying loads. The four-leg, eight switches VSC is used as the DSTATCOM. The simulation results have proved the fast and effective response for the extraction of fundamental component of load currents for harmonic compensation, load balancing, neutral current compensation and power factor / reactive power compensation with a limit of IEEE - 519 -1992 standard guidelines. The proposed SOGI controller is taking less computational burden and has proved its effectiveness in mitigating source-neutral current and the DC bus voltage is regulated compared with the reference and power factor is also improved as expected. The dynamics and efficiency confirms the potential for implementing in real-time applications.

APPENDIX

AC supply source	3-Phase, 415 V (L-L)
Frequency	50Hz
Source Impedance	Rs=0.05 Ω, Ls =2mH
Non-linear: Three phase full bridge uncontrolled rectifier	R=24 Ω, L= 80mH
Non-linear: Single phase full bridge uncontrolled rectifier	R=50 Ω
Rating of VSC	12 KVA
Ripple filter	Rf = 5Ω, Cf =7μF
Switching frequency	8kHz
Reference dc bus voltage	720V
Interfacing inductor	Ls=5mH
Gains of PI controller for dc bus	*kpt* =2, *kit*=0.3
Cut off frequency of low pass filter used in dc bus voltage	45Hz
Cut off frequency of low pass filter used in ac bus voltage	16Hz
Gains of PI controller for AC bus	*kpt* =0.2, *kit*=0.3

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