IMPLEMENTATION OF VSBSMC plus PDIC FOR FUNDAMENTAL POSITIVE OUTPUT SUPER LIFT-LUO-CONVERTER

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Abstract:-*This article studies a design and implementation of variable structure based sliding mode controller (VSBSMC) plus proportional double integral controller (PDIC) for output voltage regulation of the fundamental positive output super lift Luo-converter (FPOSLLC) operated in continuous conduction mode (CCM). Because of non-linear ON/OFF nature of the FPOSLLC and their dynamic characteristics is poor. In order to increase the dynamic characteristics and output voltage regulation of the FPOSLLC, a VSBSMC plus PDIC is developed. The designed VSBSMC plus PDIC is more appropriate to the naturally variable-structured FPOSLLC, when expressed in the state-space average model. The performance of the designed controller is demonstrated for its robustness to perform over a wide range of working conditions through both in MATLAB/Simulink model and in the experimental model with the comparative study of a VSBSMC plus proportional integral controller (PIC). The results have showed that the VSBSMC plus PDIC can achieve outstanding output voltage and inductor current regulations for FPOSLLC at various states.*

Key words: *DC-DC converter, super lifts Luo-Converter, linear controller, SMC, state-space average model*

I. INTRODUCTION

In recent days, the dc-dc conversion topologies are developing very fast, and it is more suitable for many applications such as power supply in various medical equipment, telecommunication network, computer peripheral equipments, data transfer equipments in robot systems, mobile phones, renewable energy power systems, etc.,[1]-[3]. The super lift technique has been successfully employed in the design of dc-dc converters, in which the output voltage transfer gain raises stage-by-stage in geometric series [4]. The fundamental positive output super lift Luo-converter (FPOSLLC) do the similar with a simple arrangement. The FPOSLLC converts positive dc input voltage into positive dc load voltage. The intrinsic worth of FPOSLLC has high gain, good performance, and small output capacitor voltage as well as coil current ripples over conventional dc-dc converters has been reported [5-8]. Normally, the FPOSLLC have complex non-linear model with parameters dissimilarity. The control methodology for such topologies needs to be studied for the future application. Therefore, in this article a FPOSLLC is chosen for study. The switching signal flow graph (SFG) and state space averaging approaches have been most broadly adopted the modeling approaches for dc-dc converters [9-11]. The deriving the equations of SFG method are uncomplicated, except a dynamic characteristic is still limited as the high frequency components are averaged out in the modeling technique. This will make the controller not fit for large-signal dynamic control. The analysis of dc-dc converters with variable structure sliding mode controller (VSBSMC) has been reported [12]. However, it could not expect the dynamic response of a switching converter in saturated region and works only for a particular optimal condition. The

implementation of linear proportional-integral-derivative (PID) or proportional-integral-controller (PIC) for the outer voltage control of many dc-dc converters has been well presented [13-15]. However, these are incredibly perceptive to circuit elements disparities, change in operating state, line and load disturbances etc. The success of non-linear controller lies in performing better against these problems as dc-dc converters are innately changeable structure systems. The controller of converters must cope with their intrinsic nonlinearity and wide input voltage and load disturbances. A VSBSMC make sure stability in at all working condition while providing fast transient and improved dynamic responses. Primarily, the VSBSMC (non-linear controller) utilizes a high-speed switching control law to drive the nonlinear state trajectory onto a particular surface in the state space, called the sliding or switching surface, and to sustain it on this surface for all succeeding time [16-20].

Literature Surveys: Utilization of VSBSMC at multiplicity of sliding surfaces for dc-dc converters has been presented [21]. The reduced order based fixed/variable switching frequency non-linear controller for negative super lift Luo-converter has been well addressed [22, 23]. However, this article has presented the control of output voltage and inductor current for selection of single integral based sliding surface that produced the more steady state error, large start-up settling time of the response and large overshoots during the dynamic conditions, and also difficulty controller implementation. The reduced order based VSBSMC for Cuk' dc-dc converter has been dealt [24]. Still, this article has studied the regulation of output voltage and supply current for this converter using VSBSMC that are produced more start-up overshoots in start-up as well as in dynamic working regions. Current distribution control for paralleled FPOSLLCs and output voltage regulation of voltage lift Luo-converter using variable frequency based VSBSMC without order reduction method has been reported [25, 26]. Still, these articles has studied the regulation of output current and voltage for the sensing of all state variables of the converters parameters to form the sliding surface for the controller that will make the large number of sensors, more calculations and more overshoots in dynamic performance in line and load changes. The fixed switching frequency based SMC for higher-order dc-dc converters have been addressed [27, 28]. Yet, this control method has more calculations, complex implementation and needs of larger sensors for sensing the circuit feedback variables. The design SMC for single ended primary inductance converter (SEPIC) has been reported [29, 30]. Still, the results of such article have been produced poor dynamic performance and needed more number of sensing units. These problems are solved by the designed VSBSMC plus proportional double integral controller (PDIC).

Therefore, in this article, it is proposed to a sliding surface design of VSBSMC plus PDIC for FPOSLLC worked in continuous conduction mode (CCM). The state-space average model for FPOSLLC is derived at first and then VSBSMC plus PDIC is developed. The performance analysis's of the FPOSLLC using designed VSBSMC plus PDIC is verified at different operating regions through proper selection of sliding surface coefficients of the controller. This idea and effort of implementing a VSBSMC plus PDIC for VSS in an analog platform will be a valuable contribution to researchers working in this area and also a simple solution to the problems connected with the conventional VSBSMC. The tuning of PDIC parameters are obtained with help of Ziegler Nichol's tuning method. The main significances of designed VSBSMC are realization with variable frequency (within the boundary band limit), simple control structure, small computation, simple implementation of control method and small number of sensing devices used in control prototype model. The organization of this article is as follows. Section 2 presents the operation, modeling, and design calculation of the FPOSLLC. The design procedure of VSBSMC plus PDIC for FPOSLLC is presented in section 3. The results of FPOSLLC using controllers are discussed in sections 4. The conclusions are listed in section 5.

2 Working and Modeling of FPOSLLC

2.1 Circuit description, operation and state space average model

The power circuit of the FPOSLLC is depiction in Fig.1 (a). The resourceful voltage step-up capability can be obtained by controlling the power switch Q of the FPOSLLC. In the power circuit, V_{in} is a dc input supply voltage, Q is the power switch (n-channel MOSFET) and (D_1, D_2) are freewheeling diodes. The energy storage passive elements are capacitors (C_1, C_o) and inductor L_1. V_O is the output voltage and R is the load resistance. It is assumed that all the components are ideal and also the FPOSLLC operates in CCM. To analyze the working of the FPOSLLC, the circuit can be divided into two modes, viz. the switch-ON and the switch-OFF. Fig.1 (b) and Fig.1(c) show the two modes of operation of the FPOSLLC [4]. In mode 1 operation, when the switch Q is ON, the diode D_1 conducts. The capacitor C_1 is charged with supply voltage V_{in} in short span of time period and this capacitor voltage is assumed a steady value. The current through the inductor i_{L1} rises with V_{in}. The output capacitor, C_o provides the energy to the output load. The equivalent circuit of FPOSLLC in state 1 operation is shown in Fig. 1(b). The state space equation can be engraved as (1)

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_{in} \\ C_o \dfrac{dV_o}{dt} = -\dfrac{V_o}{R} \end{cases} \quad \text{Switch ON} \qquad (1)$$

During the state 2 operation, switch Q is in OFF state, diode D_2 conduct and hence, the inductor current decays with voltage of - (V_o - 2V_{in}) to offer energy to C_o and R. The equivalent circuit of FPOSLLC in state 2 is shown in Fig.1(c). The state space equation of can be written as (2)

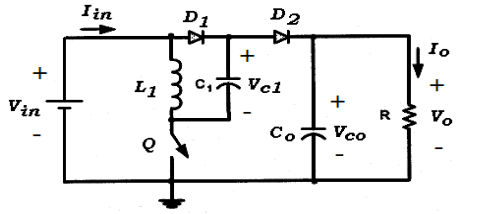
$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = 2V_{in} - V_o \\ C_o \dfrac{dV_o}{dt} = i_{L1} - \dfrac{V_o}{R} \end{cases} \quad \text{Switch OFF} \qquad (2)$$

Using the capacitor charge balance rule on C_1, the equation (3) for whole switching time period can be written.

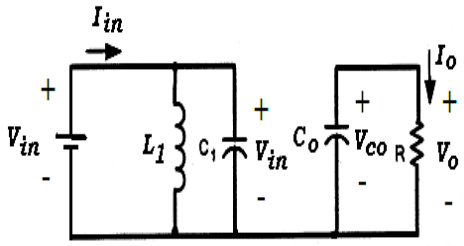
$$dC_1 \frac{dV_{C1}}{dt} + (1-d) i_{L1} = 0 \qquad (3)$$

Where, d is duty cycle.

The inductor current i_{L1}, and voltage v_o respectively x_1, and x_2. Using (1), (2), (3), and also considering d = 1 when the Q is the conduction subinterval, as well as d = 0 after the diode is the on-state subinterval, the modeling of the FPOSLLC may be reached as expressed by (4)



(a)



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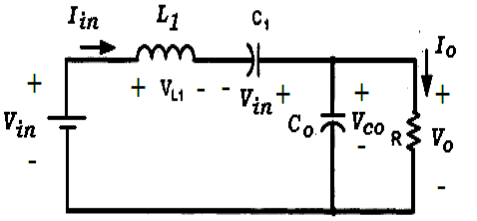


(c)

Fig.1 The power circuit of FPOSLLC (a) Topology, (b) Equivalent circuit in mode 1, and (c) Equivalent circuit in mode 2.

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\ \dfrac{1-d}{C_o} & -\dfrac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} + \begin{bmatrix} \dfrac{2-d}{L_1} \\ 0 \end{bmatrix} V_{in}$$

$$Y = [0 \quad 1] \begin{bmatrix} i_{L1} \\ V_o \end{bmatrix} \qquad (4)$$

$$A = \begin{bmatrix} 0 & -\dfrac{1-d}{L_1} \\ \dfrac{1-d}{C_o} & -\dfrac{1}{RC_o} \end{bmatrix}, \quad B = \begin{bmatrix} \dfrac{2-d}{L_1} \\ 0 \end{bmatrix}, \qquad (5)$$

$$C = [0 \ 1], \ D = [0 \ 0]$$

Where, *A, B, C* and *D* are averaged system state space matrices.

2.2 Design computation of FPOSLLC components

The FPOSLLC parameters are developed with the pursuing specifications as recorded in Table 1.

The design parameters are substituted in (4) and then apply the phase-variable transformation, *A, B, C* and *D* matrices becomes

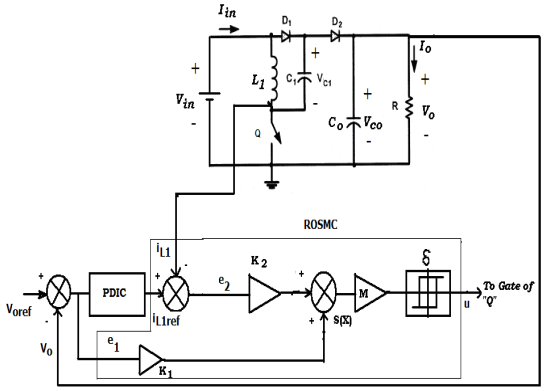
$$A=\begin{bmatrix}0 & -5000\\ 11000 & -666.67\end{bmatrix},\quad B=\begin{bmatrix}0\\1\end{bmatrix},\qquad (6)$$
$$C=[165000000 \quad 0],\ D=[0\ \ 0]$$

Table 1.Specifications of the FPOSLLC

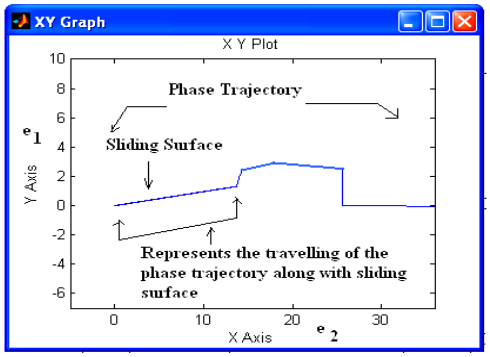
Parameters name	Symbol	Value
Input Voltage	V_{in}	12V
Output Voltage	V_o	36V
Inductor	L_1	100µH
Capacitor	C_1, C_0	30 µF
Nominal switching frequency	f	100kHz
Load resistance	R	50Ω
Output power	P_o	25.92W
Input power	P_{in}	28.236W
Average input current	I_{in}	2.353A
Efficiency	η	91.8%
Average output current	I_o	0.72 A
Duty ratio	d	0.667
Peak to Peak Inductor Current Ripple	Δ_{iL1}	25% of I_{in}
Peak to Peak Output Capacitor Ripple Voltage	ΔV_o	0.12V

3 Designs of Control Methods

The main aim of this section is to study about the design of controllers for FPOSLLC. The VSBSMC plus PDIC scheme for a FPOSLLC converter is shown in Fig. 2 (a).



(a)



(b)

Fig 2. Development of VSBSMC, (a) The control scheme for FPOSLLC using VSBSMC plus PDIC, (b) Simulated result of region of existence of SM in the phase plane of FPOSLLC using VSBSMC plus PDIC.

The controller is divided into two loops namely, an inner current loop that uses VSBSMC for control the inductor current, and an outer voltage control loop utilizing the PDIC to regulate the output voltage of FPOSLLC and reduced steady state error. The input to the PDIC is the output voltage error and the output sets the i_{L1ref} for inside current control loop. The inputs to the VSBSMC are output voltage error e_1 and the current error e_2. The output of VSBSMC u is the control signal, which in turn sets the new duty ratio of the switching pulse for driving the power MOSFET switch of FPOSLLC.

3.1 Mathematical design of VSBSMC

Let Y be the vector which contains dynamic variables, X be the original state variables and e be the error vector.

$$Y = \begin{bmatrix} y_1 & y_2 \end{bmatrix}^T , \; X = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^T , \; e = \begin{bmatrix} e_1 & e_2 \end{bmatrix}^T$$

Considered the actual state variables are $x_1 = i_{L1}$, $x_2 = V_o = V_{co}$, dynamic reference variables are $j_1 = i_{L1ref}$, $j_2 = V_{oref}$. The error values e_1 and e_2 are expressed as (7)

$$\begin{aligned} e_1 &= \begin{bmatrix} y_1 - x_1 \end{bmatrix} = \begin{bmatrix} V_{oref} - V_o \end{bmatrix} \\ e_2 &= \begin{bmatrix} y_2 - x_2 \end{bmatrix} = \begin{bmatrix} i_{L1ref} - i_{L1} \end{bmatrix} \end{aligned} \quad (7)$$

Using the phase-variable canonical transformation to represent the FPOSLLC while fixing the sliding surface $S\ (e,\ t)$, the state space average model of FPOSLLC in phase-variable form is expressed by (8)

$$\dot{X} = AX + Bu \quad (8)$$

Where,

$$A = \begin{bmatrix} 0 & -5000 \\ 11000 & -666.67 \end{bmatrix}, \; B = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \quad (9)$$

For a FPOSLLC, the $S\ (e,\ t)$ is defined as the linear function of tracking vector and is given by (10)

$$S\ (e,t) = \begin{bmatrix} K \end{bmatrix} [e] \quad (10)$$

Where, co-efficient vector $K = \begin{bmatrix} K_1 & K_2 \end{bmatrix}$ and $K_1 , \; K_2 \rangle 0$

The objective of the tracking error problem is to keep the error vector *(e)* always on the sliding surface $S\ (e,\ t) = 0$, which implies that the error signal converges exponentially to zero and is engraved by (11).

$$\dot{S}\ (e,t) = \begin{bmatrix} K \end{bmatrix} \begin{bmatrix} \dot{e} \end{bmatrix} = 0 \quad (11)$$

On the sliding surface, a second-order system model is reduced to first-order system model with stable linear differential equation. In addition, the system dynamics on the sliding surface is computed only by the controller co-efficient vector *K*. Thus, the control is insensitive to parameter variations. To calculate the control law, the error state space equation using the nearby states is derived as indicated in (12) and (13).

$$\dot{e} = \dot{Y} - \dot{X} \quad (12)$$

$$\dot{e} = \dot{Y} - AX + Bu \quad (13)$$

Substituting X = Y – e in (13), $\dot{e}$ is expressed as

$$\dot{e} = \dot{Y} - AY + Ae - Bu \quad (14)$$

The Filippov's average equivalent switch control u_{eq} that guarantees the $\dot{S}(e,t) = 0$ is found as

$$\dot{S} = Ke = \begin{bmatrix} K \end{bmatrix} \begin{bmatrix} \dot{Y} - AY + Ae - Bu_{eq} \end{bmatrix} = 0 \quad (15)$$

The value of control signal is found by using the above equation and it can be expressed as

$$u_{eq} = \begin{bmatrix} KB \end{bmatrix}^{-1} K \begin{bmatrix} \dot{Y} - AY + Ae \end{bmatrix} \quad (16)$$

Substituting the (14) into (16) gives the system error dynamics signals as

$$\dot{e} = \dot{Y} - AY + Ae - B(KB)^{-1} K \begin{bmatrix} \dot{Y} - AY + Ae \end{bmatrix}$$

$$\dot{e} = \begin{bmatrix} I - B(KB)^{-1} K \end{bmatrix} \begin{bmatrix} \dot{Y} - AY + Ae \end{bmatrix} \quad (17)$$

By applying invariance condition $\begin{bmatrix} \dot{Y} - AY \end{bmatrix} = 0$, the above equation is simplified as

$$\dot{e} = \begin{bmatrix} I - B(KB)^{-1} K \end{bmatrix} Ae = A_{eq} e \quad (18)$$

If $(KB)^{-1}$ exists, the vector *K* is derived by choosing the eigen values of A_{eq} such that it guarantees the asymptotic convergence of error to null on the expected value. The matrix A_{eq} is selected to satisfy (18) and is expressed as

$$A_{eq} = \begin{bmatrix} -0.904 & 0 \\ 0 & -0.099 \end{bmatrix}$$

The values of matrix *K* is then found using (18) as

$$K = \begin{bmatrix} K_1 & K_2 \end{bmatrix} = \begin{bmatrix} 1 & 0.09 \end{bmatrix} \quad (19)$$

Thus, the sliding surface *S* is given by

$$S = K_1 e_1 + K_2 e_2 \quad (20)$$

The (20) indicates that if the FPOSLLC works in sliding mode (when $S = 0$, stability condition), the dynamics of errors e_1 and e_2 be possible exponentially to zero with a time constant ratio of K_1 / K_2. While in the step transient's period, the FPOSLLC is in reaching mode, and therefore for this use K_1 and K_2 are computed to be in 1 and 0.09, respectively. Also the (18) describes the error action under VSBSMC. Once the sliding surface $S\ (e,\ t) = K\ e$ is designed then the control law for hitting condition is defined as

$$u = M\ sgn(S)x_2 = Ux_2 \quad (21)$$

Where, hitting or reaching conditions

$$U = 1 \quad for\ S > \delta$$
$$U = 0 \quad for\ S < \delta .$$

In this work, δ = 0.05 is selected by trial and error iterative method. The (21) is applied to generate the gate pulse to drive power MOSFET of FPOSLLC, which in turn regulate dc output voltage, steady state error and inductor current. In this work, M is constant number and equal to unity so that $S\acute{S} < 0$ (existence condition is satisfied). The reaching condition ensures that the tracking error trajectory is asymptotically involved to $S = 0$ (stability condition). It is showed that the (21) does not depend on the working regions, system parameters and limited disturbances. This is reached providing the control input u is more adequate to sustain the FPOSLLC subsystem in stable region.

$$S(X) = X_1 + K_2 X_2 \quad (22)$$

Where, $K^T = [1, K_2]$ is the vector of sliding surface coefficients which correspond to K in (16)

$$\dot{S}(X) = \begin{cases} K^T AX + K^T BU^+ + C^T D, & for\ S(X) > 0 \\ K^T AX + K^T BU^+ + C^T D, & for\ S(X) < 0 \end{cases} \quad (23)$$

After substituting the values of A, B, C, D and K, the above equation can be expressed by

$$S_1(X) = 11000K_2X_1 - 5000K_1X_2 - 666.67K_2X_2$$
$$S_2(X) = 11000K_2X_1 - 5000K_1X_2 - 666.67K_2X_2 + K_2 \quad (24)$$

Equations $S_1(X) = 0$ and $S_2(X) = 0$ define two lines in the state plane with the similar slope going through the zero. These equations represent the sliding surface for Q-ON mode and OFF mode conditions that are limited to one the sliding surface of a FPOSLLC using a VSBSMC plus PDIC for K_1, K_2 is shown in Fig. 2 (b). From this phase trajectory, it is clearly observed that the suitable value of K_2 controls the dynamic response of the system proficiently. When the phase trajectory is above the sliding surface, the Q is turned off state (U= 0) and when the phase trajectory is below the sliding surface, the switch is turned on state (U=1).

3.2 Design of PDIC

The output voltage of the FPOSLLC is controlled using PDIC. The V_o is measured and compared with desired V_{oref} that offers the voltage error signal. This error signal is applied to the PDIC to keep the V_o fixed as well as minimize the steady state error. In this article, the PDIC output sets the i_{Lref} for inside current loop. The parameters of this controller like proportional gain (K_p) and double integral times (T_is), are determined with knowledge of the Zeigler–Nichols tuning procedure [13]-[16]. The transfer function G(s) of equation (25) is obtained from state space average model of equation (4) using matrix laboratory. After that,

$$G(s) = \frac{2.274e^{-13}\ s + 1.65e^8}{s^2 + 666.7\ s + 5.5e^7} \quad (25)$$

For simplicity in the design aspect, the term $2.274e^{-13}$s in the numerator of the T.F model is very small and hence it can be neglected. Therefore, the T.F becomes

$$G(s) = \frac{1.65e^8}{s^2 + 666.7\ s + 5.5e^7} \quad (26)$$

The characteristics equation with proportional control is expressed by

$$S^2 + 666.7\ s + (5.5e^7 + K\ 1.65e^8) = 0 \quad (27)$$

The routh array of equation (45) is

S^2 : 1 $\quad (5.5e^7 + 1.65\ e^8\ K)$

s : 666.7

s^0: $(5.5e^7 + 1.65\ e^8 K)$

From this method, the system is providing a sustained oscillation with ultimate gain for stability can be obtained by use of the Routh-Hurwitz condition (K_{cr} = 0.02) and its corresponding ultimate period (P_{cr} = 0.00012s). Using this method the values of $K_p = K_{cr}/2$=0.01 and T_i s = P_{cr} /1.2=0.0011s (obtained value) and 0.00621s (which is chosen based on the observation of the system response trial-error method) are found.

4 Simulation and Experimental Results

The main aim of this section is to discuss about the experimental and simulation results of the FPOSLLC with designed controllers. The corroboration of the system performance is done for various conditions. The experimental prototype and Simulink simulation

models are performed on the FPOSLLC circuits with specifications cataloged in Table 1. The experimental prototype model of the FPOSLLC with the implemented VSBSMC plus PDIC is shown in Fig.3. The details of the power circuits are as follows:

Q	IRFN 540 (MOSFET);
D_1 - D_2	FR306 (Diodes);
$C_1 - C_O$	30 µF/100V (Electrolytic and plain polyester type)
L_1	100µH/5A (Ferrite Core)

The parameters of the controller are: K_1 =1, K_2 = 0.09, δ = 0. 05 K_p = 0.01, T_i s =0.0011s and 0.00621s as calculated in the previous section. The designed VSBSMC plus PDIC is implemented in analog platform as shown in Fig. 3. and its functionality as follows; the inductor current, output voltage V_o of FPOSLLC are sensed with help of LTS 25 – NP hall-effect current sensor, and resistances. The measured output voltage of FPOSLLC is compared with reference output voltage signals by using TL084 operational amplifier and it provides the error signal and this error signal is processed through the PDIC to generate the reference current which is compared with the measured circuit inductor current and this will offer current error signal. Further, both the current and the voltage errors are processed through the sliding surface coefficients and its outputs are added to structure the sliding surface using TL084 operational amplifiers. This sliding surface signals are compared using TL071 to generate the pulse width modulated (PWM) gate drive control signal of power switch. The hysteresis upper and lower band limits are constructed by using the TL071, flip-flop 4013, logical AND gate, and N E 555 (these components are used to generate and set the 100 kHz operating frequency for proposed model). After, the generated gate signal is passed through the op-isolator (6N137), driver IC 2125, and resistances arrangement. The output of the driver is linked with the MOSFET gate (IRFN 540) as shown in Fig. 3. Using the VSBSMC plus PDIC, the switching frequency of gate pulse is varied to regulate the output voltage, inductor current and enhance the transient, reduced steady state errors and increases dynamic characteristics of FPOSLLC.

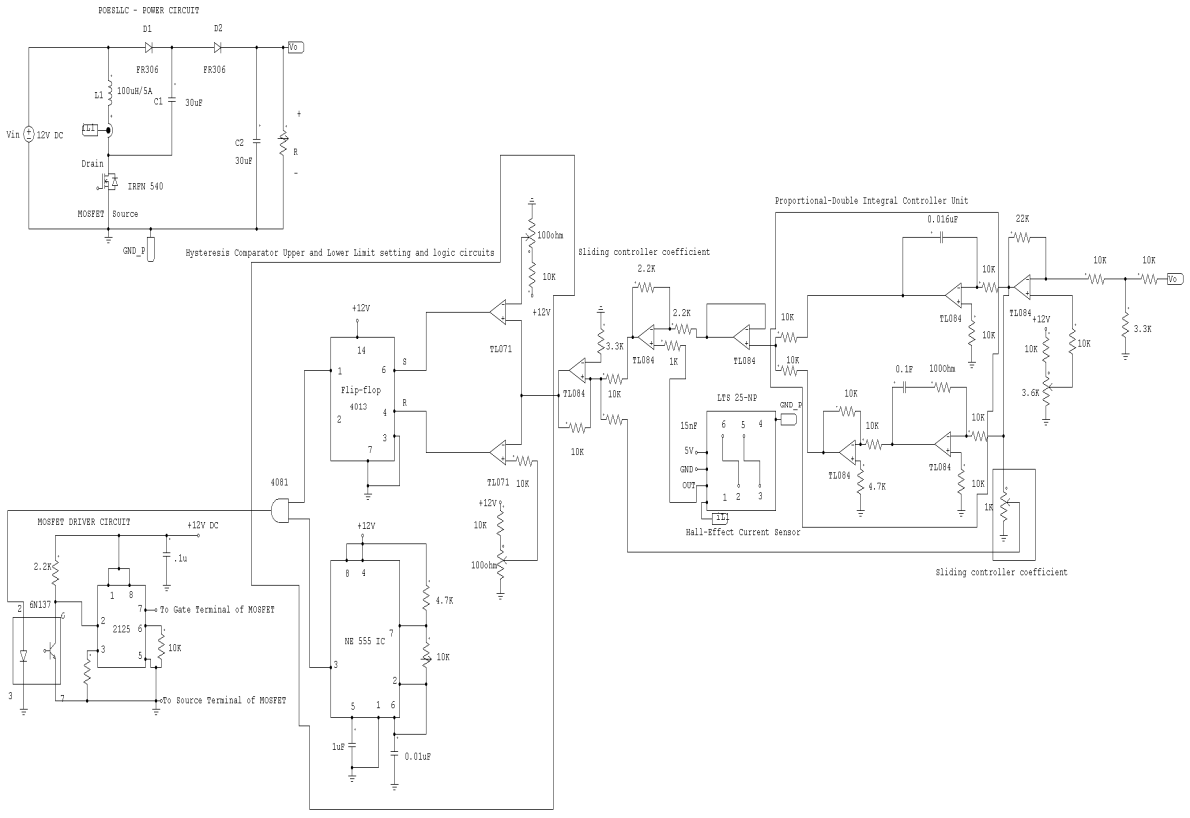
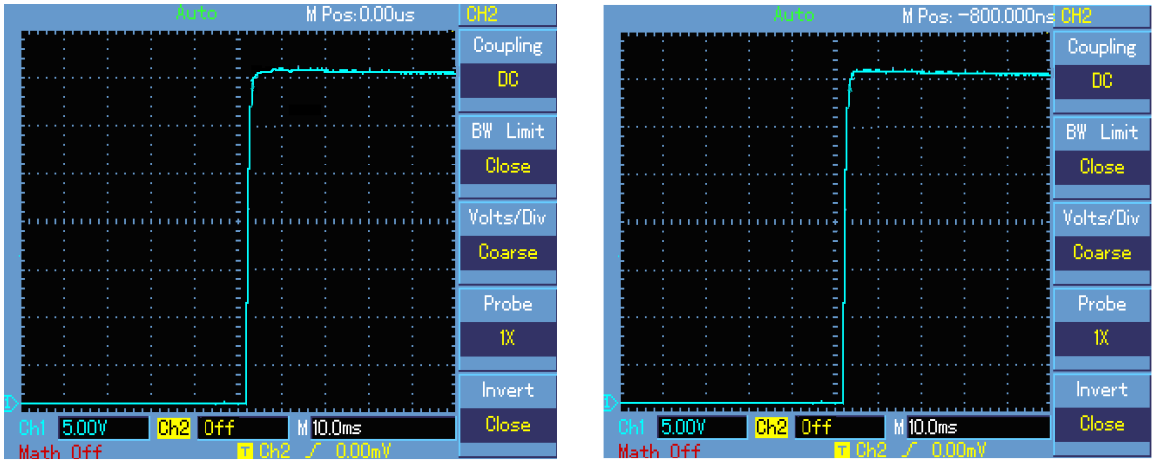
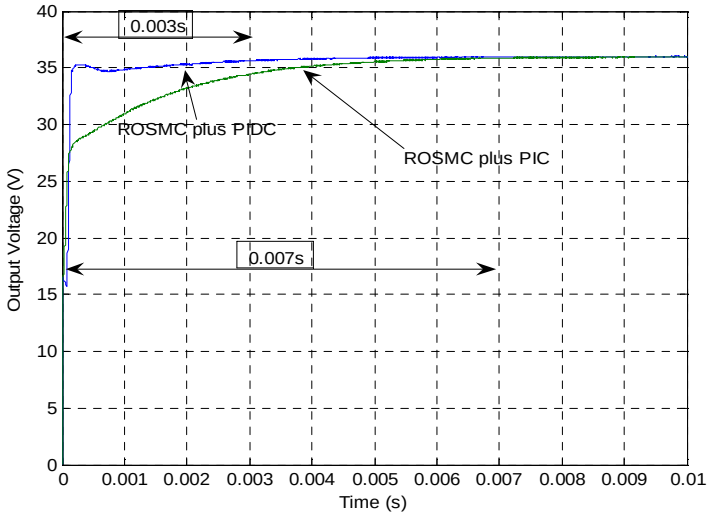


Fig 3. Experimental model of the FPOSLLC using a VSBSMC plus PDIC /PICin analog platform.



(a) (b)



(c)

Fig 4. Experimental startup response of output voltage of FPOSLLC in time domain, (a) using VSBSMC plus PDIC [Ch1:5V/Div-output voltage], (b) using VSBSMC plus PIC [Ch1:5V/Div-output voltage], and (c) simulated start-up output voltage of FPOSLLC using VSBSMC plus PDIC and VSBSMC plus PIC.

4.1 Start-up transient

Fig.4 (a) illustrates the experimental dynamic behavior in terms of the output voltage start-up of the FPOSLLC for input voltages 12V using designed controller. It can be indicated that output voltage of the FPOSLLC using VSBSMC plus PDIC has a negligible start-up overshoot and settling time of 0.0035s for V_{in} = 12 V. Fig.4 (b) shows the experimental output voltage start-up for input voltages 12V using VSBSMC plus PIC. It is seen that output voltage of the FPOSLLC using this control scheme has a slightly overshoot and settling time of 0.008s for V_{in} = 12 V. Fig. 4(c) depicts the simulation responses of the output voltage start-up of FPOSLLC using both control schemes. From this figure, it can be found that the output voltage of converter using VSBSMC plus PDIC has quick settling time (0.003s) and negligible overshoot, whereas the output voltage of same converter using VSBSMC plus PIC has settled long time (0.007s) and null overshoot.

4.2 Line Variation

Fig.5(a) depict the experimental and simulation responses of the output voltage, inductor current and input voltage of the FPOSLLC using the VSBSMC plus PDIC for input voltage step change from 12V to 15V (+30% line variations) at time = 0.05s. From this figure, it is clearly found that both the experimental and simulation responses of output voltage of the FPOSLLC with the designed VSBSMC plus PDIC has overshoot of 1V and settling time of 0.006s. Fig.5 (b) show the experimental and simulation responses of the output voltage, inductor current and input voltage of the FPOSLLC using the VSBSMC plus PDIC for input voltage step change from 12V to 9V (-30% line variations) at time = 0.05s. It can be observed that both the experimental and simulation responses of output voltage of the FPOSLLC using VSBSMC plus PDIC has overshoot of 1V and settling time of 0.006s.

Fig.6(a) and (b) shows the simulated response of the output voltage of FPOSLLC using both VSBSMC plus PDIC and VSBSMC plus PIC for input voltage step change from 12V to 15V (+30% line variations) and 12V to 09V (-30% line variations) at time = 0.05s. It can be found that the output voltage of the FPOSLLC using VSBSMC plus PDIC has overshoot of (0.9V and 1.2V) and settling time of 0.006s, while the output voltage of same converter using a VSBSMC plus PIC has a severe overshoot of (2.25V and 2.6V) and a comparatively long settling time of 0.008s. From the Fig.5 and Fig.6, it is clearly identified that the simulated results of a designed VSBSMC plus PDIC are showed better performance in comparison with a VSBSMC plus PIC under the line variation.

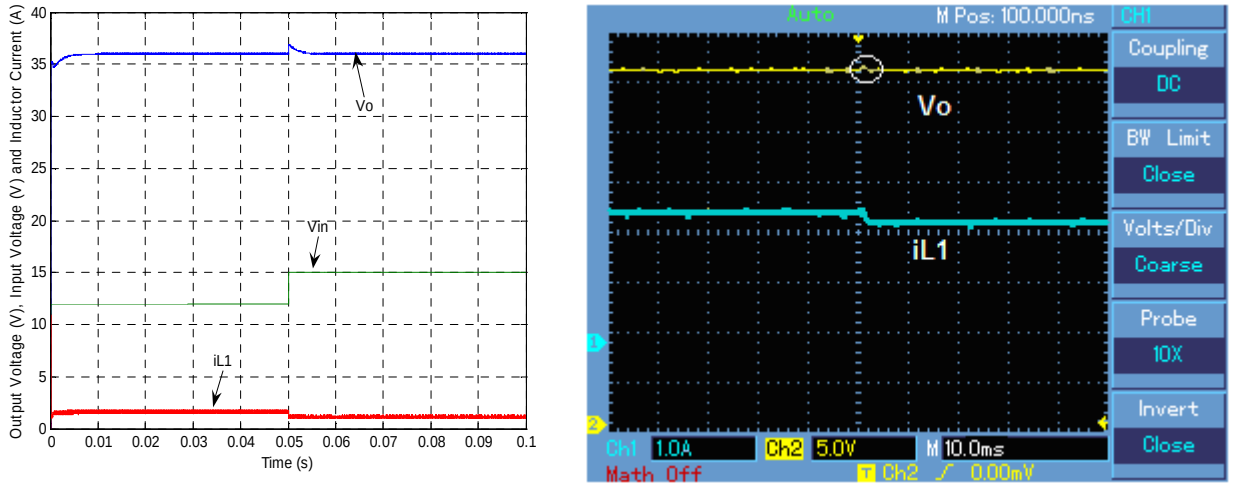
4.3 Load Variation

Fig. 7(a) and 7(b) show the experimental responses of output voltage of the FPOSLLC using both control methods for load step change 50Ω to 60Ω (+20% load variations) and 50Ω to 40Ω (-20% load variations) at time = 0.05s. It could be seen that the experimental results of output voltage of the FPOSLLC using a VSBSMC plus PDIC has a small overshoot of 0.9V with quick settling time of 0.005s, while the output voltage of converter using VSBSMC plus PIC has overshoot of 1.5V and settling time of 0.008s. Fig.7 (c) and 7(d) show the simulation responses of output voltage with the VSBSMC plus PDIC and VSBSMC plus PIC for load step change from 50Ω to 60Ω (+20% load variations) and 50Ω to 40Ω (-20% load variations) at time = 0.05s. It could be evidenced that the simulation results of output voltage of the FPOSLLC using a VSBSMC plus PDIC has a small overshoot of (0.4 V and 0.6V) with quick settling time of 0.005s, at the same time as the output voltage of converter using VSBSMC plus PIC has overshoot of (2.1V and 1.4V) and settling time of 0.008s.. From Fig.7, it is clearly understood that the experimental results reveal close agreement with simulation results under load variation for the designed VSBSMC plus PDIC.

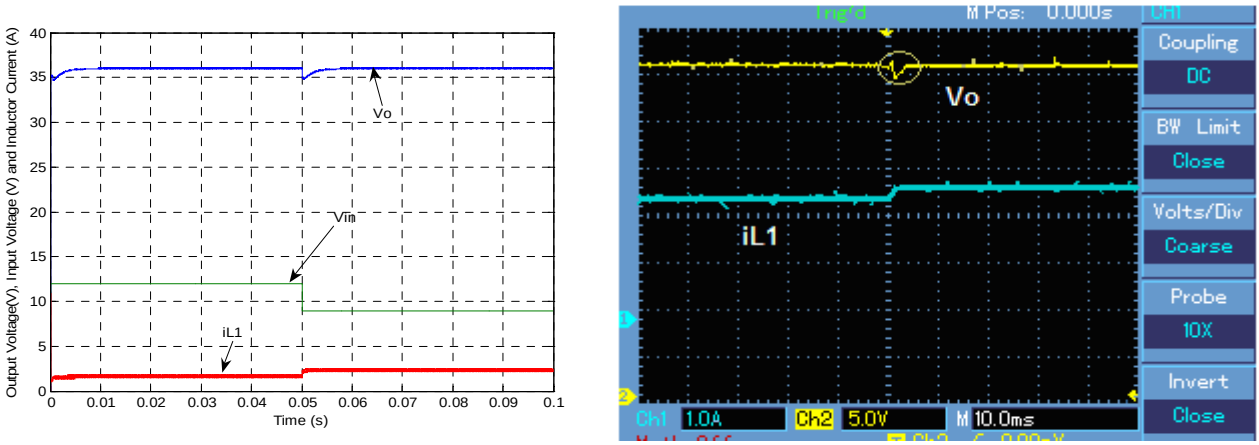
4.4 Steady state region

Fig. 8(a) shows the experimental and simulation instantaneous output voltage and the inductor current of the FPOSLLC in the steady state region using a VSBSMC plus PDIC. It is evident from the figure that the output voltage ripple is very small about 0.17V/0.05V and the peak to peak inductor ripple current is 0.3 A/0.1 A for the average switching frequency of 100 kHz closer to theoretical designed value listed in Table 1 and also it indicate that to keep the inductor current for the FPOSLLC always continuous.

Fig. 8(b) depicts the simulated instantaneous output voltage and the inductor current of FPOSLLC in the steady state region using VSBSMC plus PIC. It is evident from the result that the ripple of V_o is very little about -0.05V and the peak to peak inductor ripple current is 0.1A for the average switching frequency of 100 kHz closer to theoretical designed value listed in Table 1. Fig.8(c) show the simulated response of sliding surface of FPOSLLC using VSBSMC plus PDIC, where the sliding surface oscillates around zero. Fig. 8(d) show the graphs of the steady-state output voltage against the switching frequency of the FPOSLLC under the VSBSMC plus PDIC and VSBSMC plus PIC respectively for R= 100 ohm. From this figure, it is clearly found that the proposed controller reduces the steady-state error regulation for all values of switching frequency in comparison with VSBSMC plus PIC.

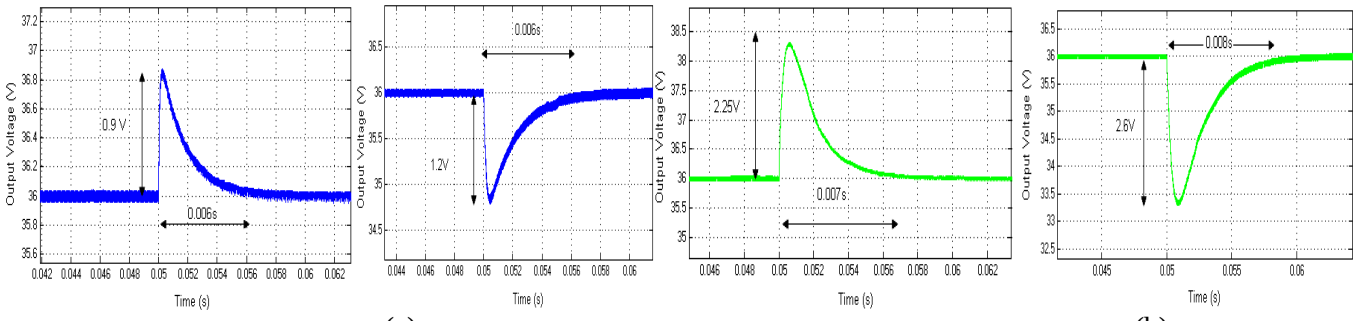


(a)



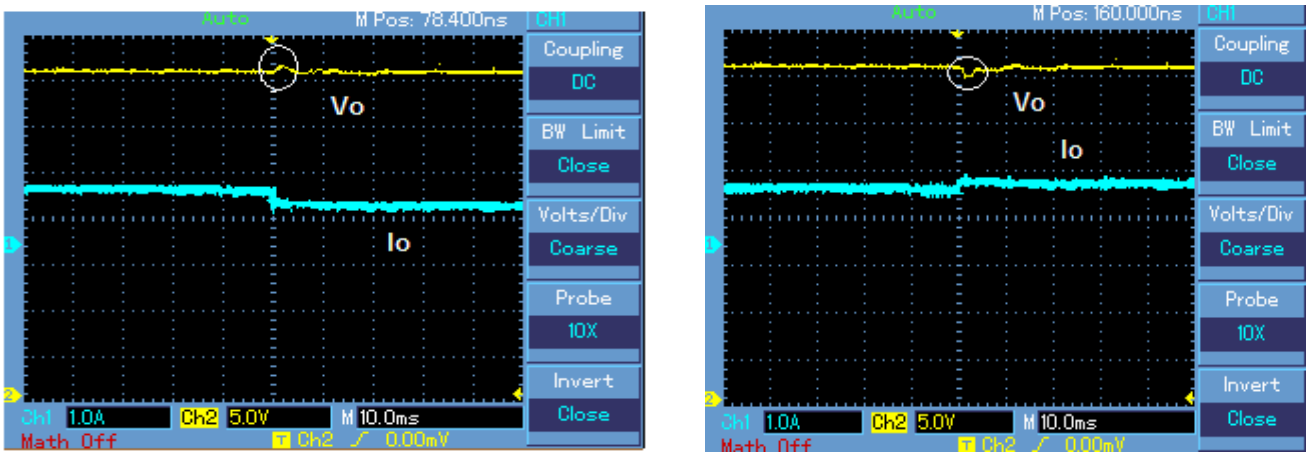
(b)

Fig 5. Simulation and experimental responses of output voltage, inductor current and input voltage of FPOSLLC with R = 50Ω, (a) for input step change from 12V to 15V at time of 0.05s using VSBSMC plus PDIC, (b) for input step change from 12V to 09V at time of 0.05s using VSBSMC plus PDIC [Ch1:1AV/Div-inductor current and Ch2:5V/Div- output voltage].

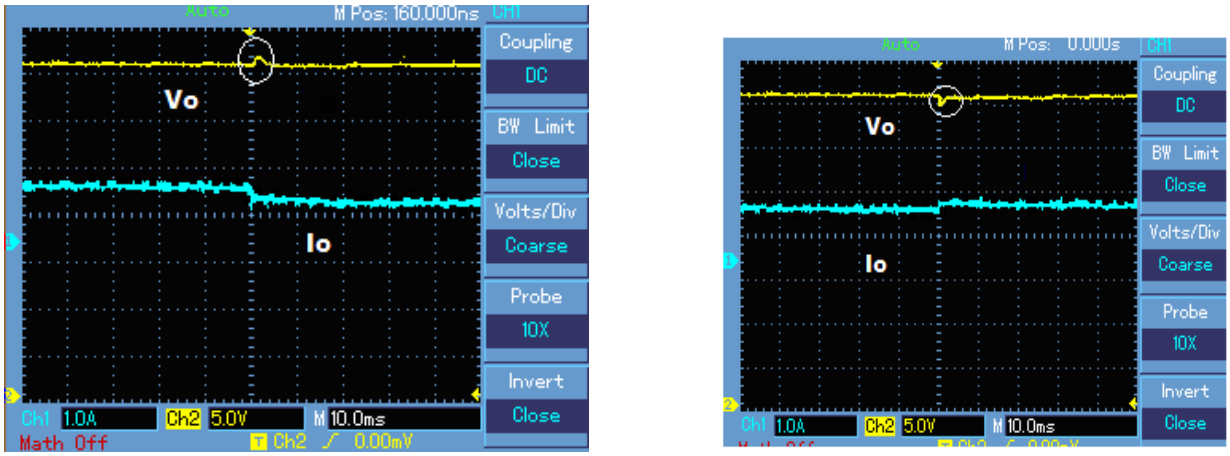


(a) (b)

Fig 6. Simulated response of output voltage of FPOSLLC for input step change from 12V to 15 V and 12 to 09V at time of 0.05s with R = 50Ω, (a) using VSBSMC plus PDIC, (b) using VSBSMC plus PIC.



(a)



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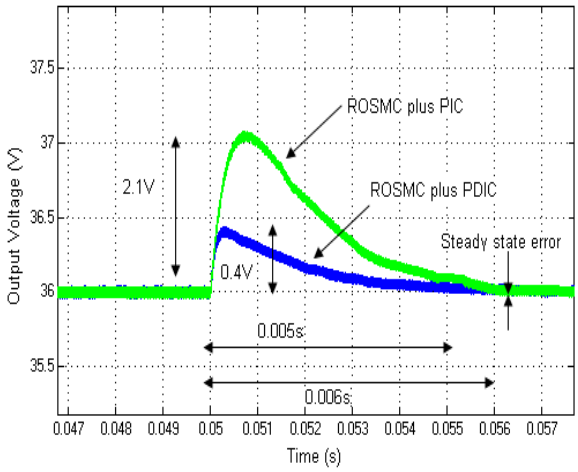
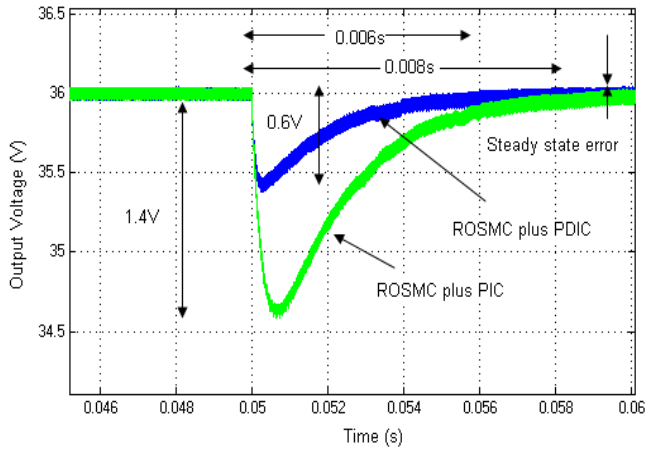
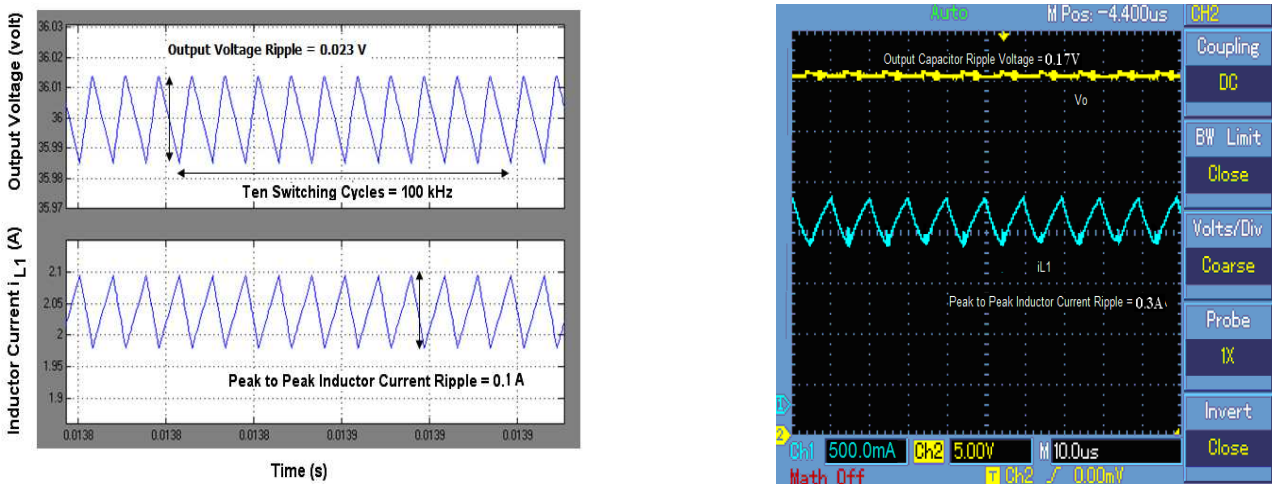


(c)

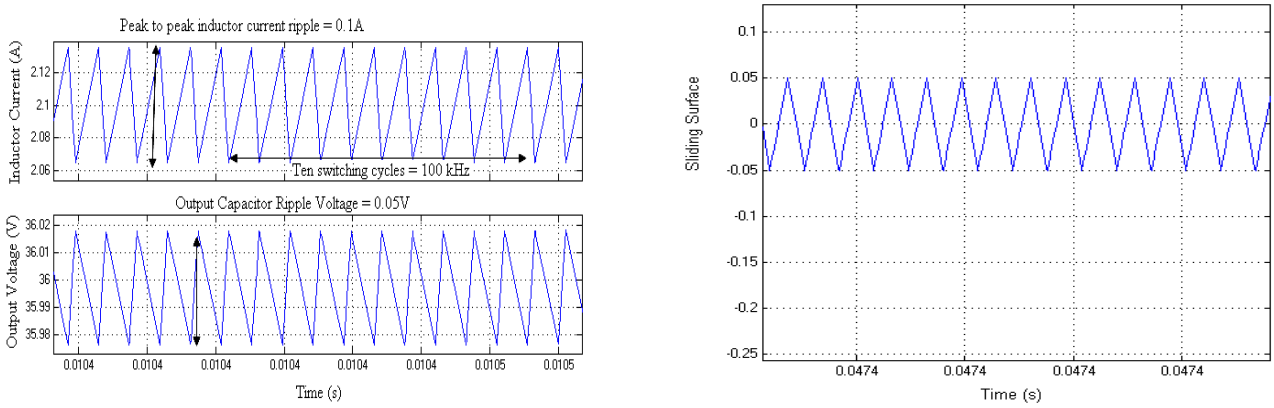


(d)

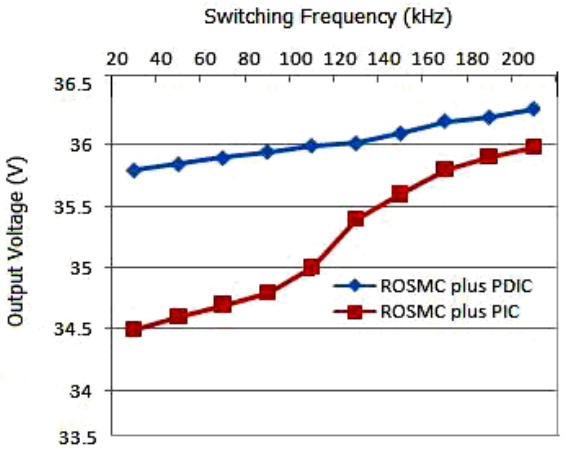
Fig 7. Experimental response of output voltage of FPOSLLC when load value takes a step changes from 50 Ω to 40Ω and 50Ω to 60Ω at time 0.05s with V_{in} = 12 V, (a) using VSBSMC plus PDIC [Ch2:5V/Div-output voltage and Ch1:1A/Div-output current], (b) using VSBSMC plus PIC [Ch2:5V/Div-output voltage and Ch1:1A/Div-output current], (c) simulated output voltage of FPOSLLC using both VSBSMC plus PDIC and VSBSMC plus PIC for load change from 50 Ω to 60Ω, (d) simulated output voltage of FPOSLLC using both VSBSMC plus PDIC and VSBSMC plus PIC for load change from 50 Ω to 40Ω.



(a)



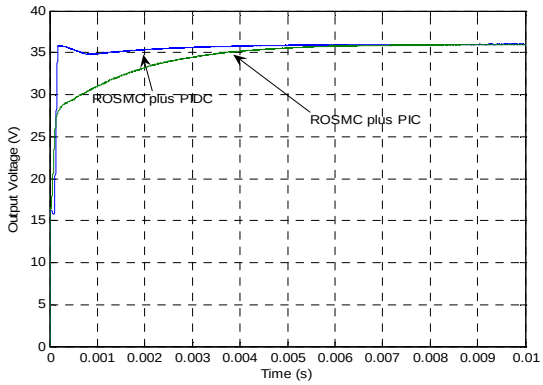
(b) (c)



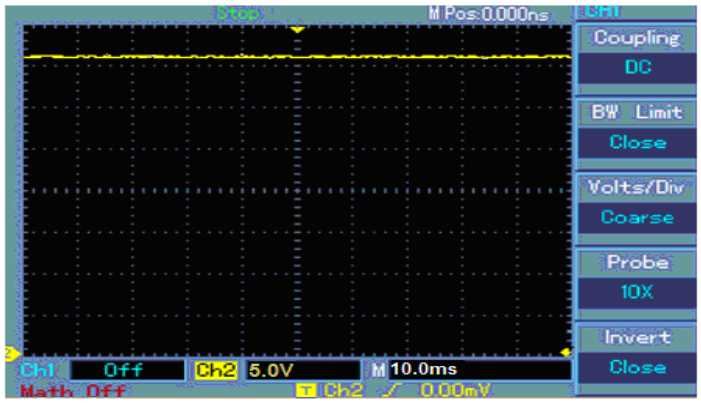
(d)

Fig 8. Experimental, simulated and graphical results of FPOSLLC in steady state condition, (a) simulated and experimental responses of output voltage and inductor current i_{L1} in steady state condition using VSBSMC plus PDIC [Ch2:5V/Div-output voltage and Ch1:500mA/Div-output current], (b) simulated response of output voltage and inductor current i_{L1} in steady state condition using VSBSMC plus PIC, (c) sliding surface in steady state condition using VSBSMC plus PDIC, (d) simulated graphical form of steady-state output voltage against switching frequency with VSBSMC plus PDIC and VSBSMC plus PIC at R=100 ohm.

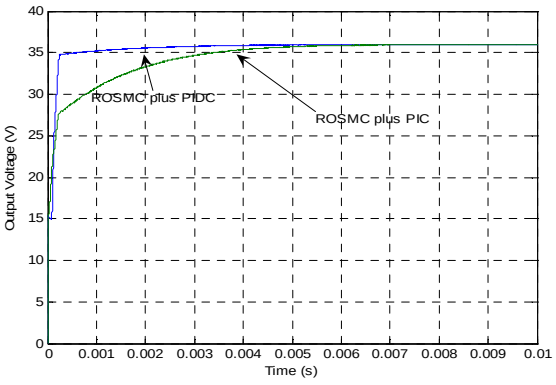
4.5 Circuit components variations



(a)



(b)



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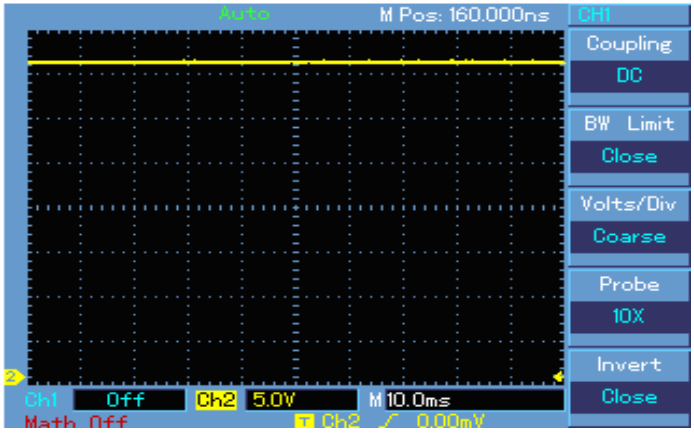
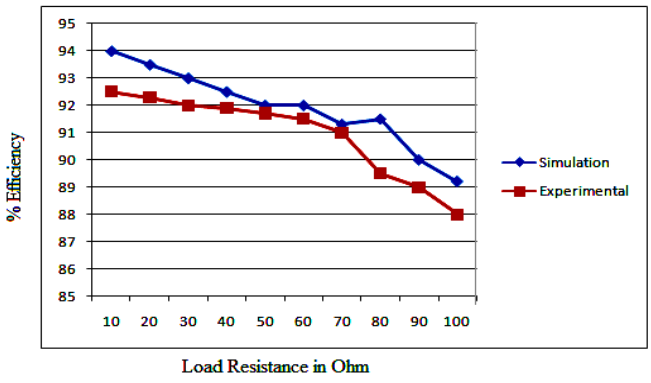
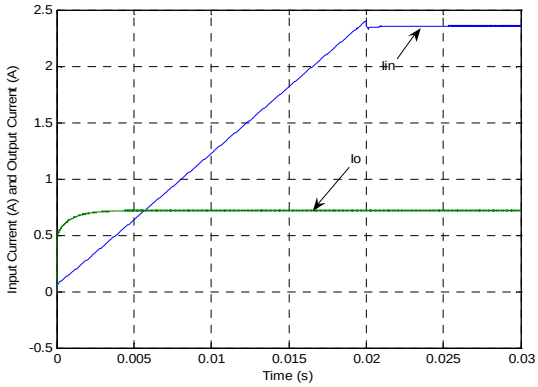


(d)



(e)



(f)

Fig 9. Circuit components variations and perforamance of FPOSLLC, (a) Response of output voltage when inductor variation from 100µH to 150µH using both controller schemes, (b) experimental response of output voltage when inductor variation from 100µH to 150µH using VSBSMC plus PDIC PDIC [Ch1:5V/Div-output voltage], (c) Response of output voltage when inductor variation from 30µF to 100µF using both controller schemes, (d) experimental response of output voltage when inductor variation from 30µF to 100µF using VSBSMC plus PDIC PDIC [Ch1:5V/Div-output voltage], (e) simulation and experimental results of % efficiency at different load conditions, (f) simulated results of average input and output current of FPOSLLC using VSBSMC plus PDIC.

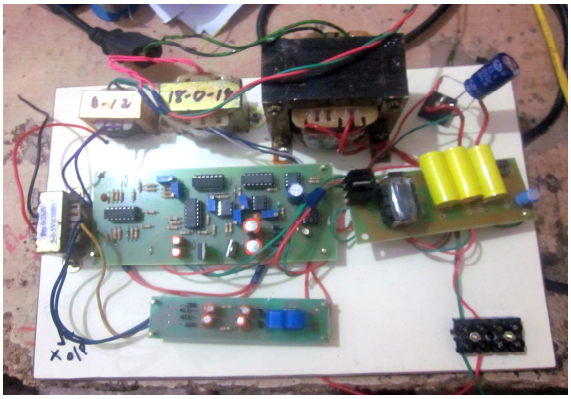


Fig 10. Photograph model of FPOSLLC using proposed controller.

Fig. 9(a) and Fig. 9(b) represent the simulation and the experimental response of output voltage of the FPOSLLC using a VSBSMC plus PDIC and VSBSMC plus PIC for inductor L_1 variation from 100µH to 500µH. It would be found that the change does not influence the FPOSLLC behaviors owing to a capable of VSBSMC plus PDIC. An attractive result is exemplified in Fig. 9(c) and Fig. 9(d). It specifies the simulation and experimental responses of output voltage of the FPOSLLC using a VSBSMC plus PDIC for the variation in capacitors values from 30µF to 100µF. It will be seen that the designed VSBSMC plus PDIC is very successful in eliminating effect of capacitors variations except that a small overshoot and quick settling time in comparison over a VSBSMC plus PIC. Fig. 9(e) indicates the graphical form of simulation and experimental results of % efficiency of the FPOSLLC using a VSBSMC plus PDIC at various load conditions. From this figure, it is clearly observed that the % efficiency of the FPOSLLC using a VSBSMC plus PIC has maintained from 87.9 % to 94.2 % at different R-stipulations. From the Fig. 5 and Fig. 9 (f), it is clearly found that the average input/output currents and input/output voltages of the FPOSLLC using a VSBSMC plus PDIC has 2.353A /0.72A and 12V/36V, that are match the theoretical designed value in Table 1. Fig. 10 indicates the photograph of laboratory prototype set-up model of FPOSLLC using designed controller. Also, the same model can be work in huge power rating with need of high level design. In summary, from the Figs. 5 to 10, it is clearly indicated that the results of the FPOSLLC using a designed VSBSMC plus PDIC match the simulated results. Finally, a designed VSBSMC plus PDIC performed well in all the working conditions of the FPOSLLC. The time domain analyzes of FPOSLLC using both controllers are listed in Table 2. From this table, it is clearly found that the designed VSBSMC plus PDIC has good performance over the VSBSMC plus PIC.

5 Conclusions

Thus, the design of VSBSMC plus PDIC using sliding surface co-efficient for FPOSLLC operated in CCM has been successfully established in MATLAB/Simulink and in analog platform. The designed VSBSMC plus PDIC has produced good output voltage inductor current responses of FPOSLLC in large variation in input supply voltage/load resistances, effortless implementation and circuit parameter variations without changing the sliding coefficients over the VSBSMC plus PIC. The simulation and experimental results are accessible to reveal the proficient of the designed VSBSMC plus PDIC for the FPOSLLC operated in CCM resulted in quick dynamic response, good regulated output voltage, and excellent output voltage in the circuit component variations, outstanding steady state and transient responses over a VSBSMC plus PIC.

It is, therefore, fit for any stable low power supply real-world commercial applications, and it is essentially intended for power source in various medical equipments, power source for computer hardware parts, telecom, and military applications and it can be extended to large-power uses.

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Table. 2. Time domain specification analysis of FPOSLLC using controllers.

Start up-Region			**Line Variations**				**Load Variations**			
Controllers	**M_p**	**T_s (s)**	**V_{in}=12Vto 15V**		**V_{in}=12Vto 09V**		**R= 50Ω to 60Ω**		**R= 60Ω to 50Ω**	
			M_p	**T_s (s)**	**M_p**	**T_s (s)**	**M_p**	**T_s (s)**	**M_p**	**T_s (s)**
VSBSMC plus PIC (Sim.)	nil	0.007	2.25V	0.008	2.26V	0.008	2.1V	0.008	1.4V	0.008
VSBSMC plus PDIC (Sim.)	**nil**	**0.003**	**1V**	**0.006**	**1V**	**0.006**	**0.4V**	**0.005**	**0.6V**	**0.005**
VSBSMC plus PDIC (Exp.)	**nil**	**0.0035**	**1V**	**0.006**	**1.2V**	**0.006**	**2.1V**	**0.008**	**1.4V**	**0.008**
VSBSMC plus PIC (Exp.)	1mV	0.008	2.26	0.008	2.26V	0.008	2.2V	0.008	1.5V	0.008